

To : LONGSE ELECTRONICS LIMITED

SPECIFICATIONS

Product Type 1/3-type Interline Color IS-CCD Area Sensor with 610k Pixels for PALModel No. R J 2 3 4 1 B A 0 P B

※ This specifications contains 21 pages including the cover and appendix.
If you have any objections, please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

DATE : _____

BY : _____

PRESENTED

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SHARP CORPORATION

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- When using the products covered herein, please observe the conditions written herein and the precautions outlined in the following paragraphs. In no event shall the company be liable for any damages resulting from failure to strictly adhere to these conditions and precautions.
 - (1) Please do verify the validity of this part after assembling it in customer's products, when customer wants to make catalogue and instruction manual based on the specification sheet of this part.

 - (2) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (3), even for the following application areas, be sure to observe the precautions given in Paragraph (3). Never use the products for the equipment listed in Paragraph (4).

Office electronics

 - Instrumentation and measuring equipment
 - Machine tools
 - Audiovisual equipment
 - Home appliance
 - Communication equipment other than for trunk lines

 - (3) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.
 - Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
 - Mainframe computers
 - Traffic control systems
 - Gas leak detectors and automatic cutoff devices
 - Rescue and security equipment
 - Other safety devices and safety equipment, etc

 - (4) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.
 - Aerospace equipment
 - Communications equipment for trunk lines
 - Control equipment for the nuclear power industry
 - Medical equipment related to life support, etc.

 - (5) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

- Please direct all queries and regarding the products covered herein to a sales representative of the company.

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1 DESCRIPTION

The RJ2341BA0PB is a 1/3-type(6.0mm) solid-state image sensor that consists of PN photo-diodes and CCDs(charge-coupled devices).

With approximately 610,000pixels (horizontal 1020 × vertical 595), the sensor provides a stable high-resolution color image.

1.1 Features

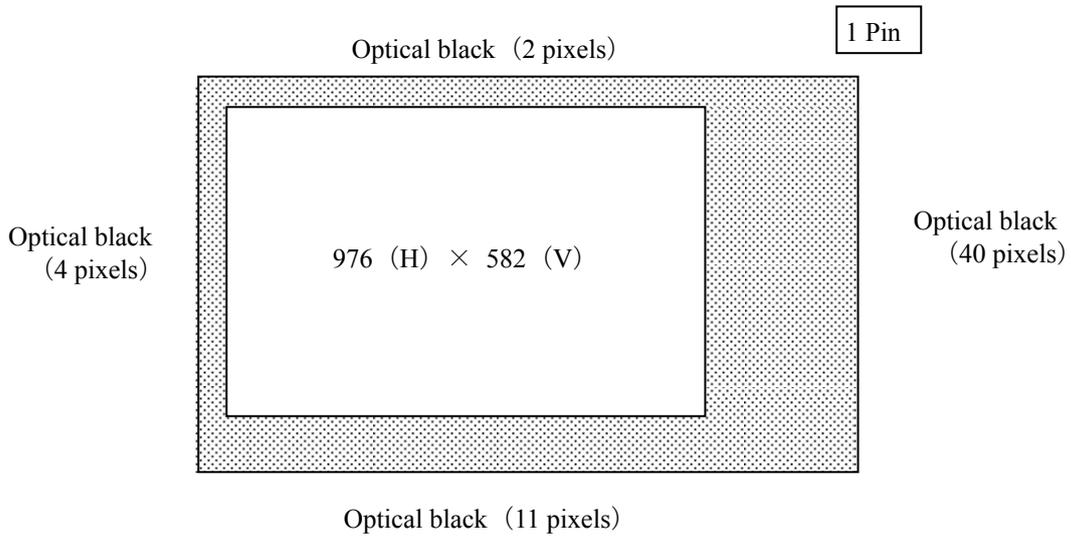
- 1) Number of image pixels : Horizontal 976×vertical 582
Pixel pitch : Horizontal 5.0 μ m×vertical 6.3 μ m
Number of optical black pixels : Horizontal ; 4 front and 40 rear
: Vertical ; 11 front and 2 rear
- 2) Mg, G, Cy, and Ye Complementary color filters
- 3) Low fixed pattern noise and lag
- 4) No burn-in and no image lag distortion
- 5) Blooming suppression structure
- 6) Built-in output amplifier
- 7) 16-pin half-pitch DIP [P-DIP016-0450]
(Row space: 11.43mm)
- 8) Variable electronic shutter (1/50 to 1/100000 s)
- 9) N-type silicon substrate, N-MOS process,
- 10) Not designed or rated as radiation hardened
- 12) Built-in overflow drain voltage circuit, and reset gate voltage circuit
- 13) Horizontal shift register clock and reset gate clock voltage : 3.3V(Typ.)

1.2 Applications

- 1) Cameras(Camcorders, industrial monitor cameras, etc)
- 2) Pattern recognition

※ The circuit diagram and others included in this specifications are intended for use to explain typical application examples. Therefore, we take no responsibility for any problem as may occur due to the use of the included circuit and for any problem with industrial proprietary rights or other rights.

2 ARRANGEMENT OF PIXELS AND COLOR FILTERS



(1, 582)

(976, 582)

Cy	Ye	Cy	Ye	Cy
Mg	G	Mg	G	Mg
Cy	Ye	Cy	Ye	Cy
G	Mg	G	Mg	G
Cy	Ye	Cy	Ye	Cy
Mg	G	Mg	G	Mg

Ye	Cy	Ye	Cy	Ye
G	Mg	G	Mg	G
Ye	Cy	Ye	Cy	Ye
Mg	G	Mg	G	Mg
Ye	Cy	Ye	Cy	Ye
G	Mg	G	Mg	G

ODD field

Cy	Ye	Cy	Ye	Cy
Mg	G	Mg	G	Mg
Cy	Ye	Cy	Ye	Cy
G	Mg	G	Mg	G
Cy	Ye	Cy	Ye	Cy
Mg	G	Mg	G	Mg

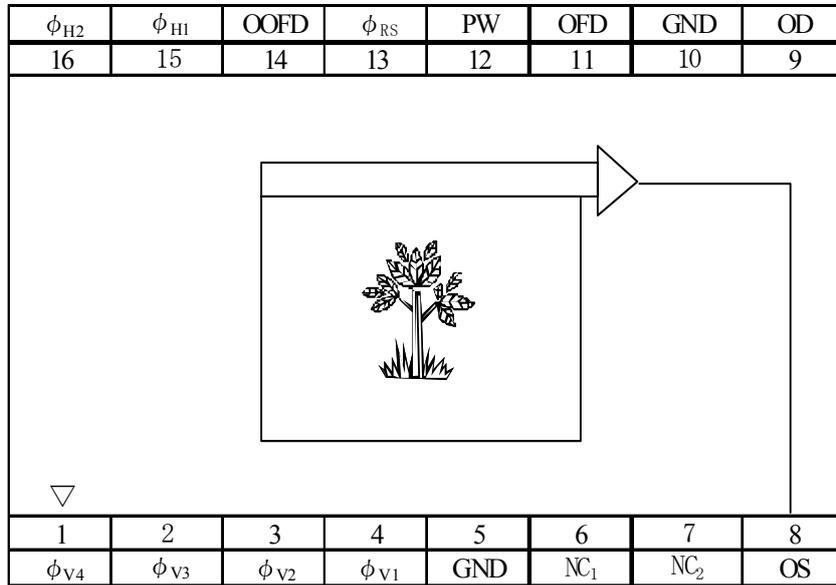
EVEN field

Ye	Cy	Ye	Cy	Ye
G	Mg	G	Mg	G
Ye	Cy	Ye	Cy	Ye
Mg	G	Mg	G	Mg
Ye	Cy	Ye	Cy	Ye
G	Mg	G	Mg	G

(1, 1)

(976, 1)

3 PIN CONFIGURATION (TOP VIEW)



(TOP VIEW)

Symbol	Pin name
OD	Output transistor drain
OS	Output signals
ϕ_{RS}	Reset transistor clock
$\phi_{V1}, \phi_{V2}, \phi_{V3}, \phi_{V4}$	Vertical shift register clock
ϕ_{H1}, ϕ_{H2}	Horizontal shift register clock
OOFD	Overflow drain
OOFD	Overflow drain output
PW	P-well
GND	Ground
NC ₁ , NC ₂	No connection

4 ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

Parameter	Symbol	Ratings	Unit
Output transistor drain voltage	V _{OD}	0 to +18	V
Overflow drain voltage	V _{OOFD}	0 to +37	V
Overflow drain output	V _{OOFD}	Internal output(Note 1)	
Reset gate clock voltage	V _{ϕ_{RS}}	Internal output(Note 2)	
Vertical shift register clock voltage	V _{ϕ_V}	V _{PW} to +17.5	V
Horizontal shift register clock voltage	V _{ϕ_H}	-0.3 to +12	V
Voltage difference between P-well and vertical clock	V _{PW} -V _{ϕ_V}	-28.0 to 0	V
Voltage difference between vertical clocks	V _{ϕ_V} -V _{ϕ_V}	0 to +1.5(Note3)	V
Storage temperature	T _{stg}	-40 to +90	°C
Ambient operating temperature	T _{opr}	-30 to +85	°C

(Note 1) Use the circuit parameter indicated in “8. STANDARD OPERATING CIRCUIT EXAMPLE” and do not connect to DC voltage directly. When OOFD is connected to GND, connect V_{OD} to GND.

(Note 2) Do not connect to DC voltage directly. When ϕ_{RS} is connected to GND, connect V_{OD} to GND. Reset gate clock is applied below 8Vp-p.

(Note 3) When clock width is below 10 μ s, and clock duty factor is below 0.1%, voltage difference between vertical clocks is will be below 27V.

5 RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typl	Max	Unit
Operating ambient temperature	Topr		25.0		°C
Output transistor drain voltage	V _{OD}	14.55	15.0	15.45	V
Overflow drain clock p-p level (Note1)	V _{φ OFD}	21.5		23.5	V
Ground	GND		0.0		V
P-well voltage (Note2)	V _{p w}	-9.0		V _{φ VL}	V
Vertical shift register clock LOW level	V _{φ V1L} , V _{φ V2L} V _{φ V3L} , V _{φ V4L}	-8.5	-8.0	-7.5	V
Vertical shift register clock INTERMEDIATE level	V _{φ V1I} , V _{φ V2I} V _{φ V3I} , V _{φ V4I}		0.0		V
Vertical shift register clock HIGH level	V _{φ V1H} V _{φ V3H}	14.55	15.0	15.45	V
Horizontal shift register clock LOW level	V _{φ H1L} , V _{φ H2L}	-0.05	0.0	0.05	V
Horizontal shift register clock HIGH level	V _{φ H1H} , V _{φ H2H}	3.0	3.3	3.6	V
Reset gate clock p-p level (Note 1)	V _{φ RSH}	3.0	3.3	3.6	V
Vertical shift register clock Frequency	V _{φ V1} , V _{φ V2A} , V _{φ V2B} V _{φ V3A} , V _{φ V3B} , V _{φ V4}		15.63		kHz
Horizontal shift register clock frequency	f _{φ H1} , f _{φ H2}		18.0		MHz
Reset gate clock frequency	f _{φ RS}		18.0		MHz

- Connect NC₁ to GND NC₂ to GND directly or through a capacitor larger then 0.047 μ F

(Note1) Use the circuit parameter indicated in “8 EXAMPLE OF STANDARD OPERATING CIRCUIT”(P 11), and do not connect to DC voltage directly.

(Note2) V_{PW} is set below V_{φ VL} that is low level of vertical shift register clock, or is used with the same power supply that is connected to V_L of V driver IC.

- To apply power, first connect GND and then turn on OD. After turning on V_{OD}, turn on V_{PW} first and then turn on other powers and pulses.
Do not connect the device to or disconnect it from the plug socket while power is being applied.

6 CHARACTERISTICS

Ambient temperature : +25°C, but +60°C for parameter No.4 and on 5.

Operating conditions : the typical values specified in “5 RECOMMENDED OPERATING CONDITION”.

Color temperature of light source : 3200K ,IR cut-off filter (CM-500,1mmt) is used.

No.	Parameter	Symbol	Note	Minimum	Typical	Maximum	Unit
1	Standard output voltage	Vo	(1)		150		mV
2	Photo response non-uniformity	PRNU	(2)			10	%
3	Saturation output voltage	Vsat	(3)	1200			mV
4	Dark output voltage	Vdark	(4)		0.5	3.0	mV
5	Dark signal non-uniformity	DSNU	(5)		0.5	2.0	mV
6	Sensitivity	R	(6)	1900	2400		mV
7	Smear ratio	SMR	(7)		-125	-105	dB
8	Image lag	AI	(8)			1.0	%
9	Blooming suppression ratio	ABL	(9)	1000			
10	Current dissipation	I _{OD}			5.0	9.0	mA
11	Output impedance	Ro			200		Ω
12	Vector breakup		(10)			5.0	°, %
13	Line crawling		(11)			1.5	%
14	Luminance flicker		(12)			2.0	%

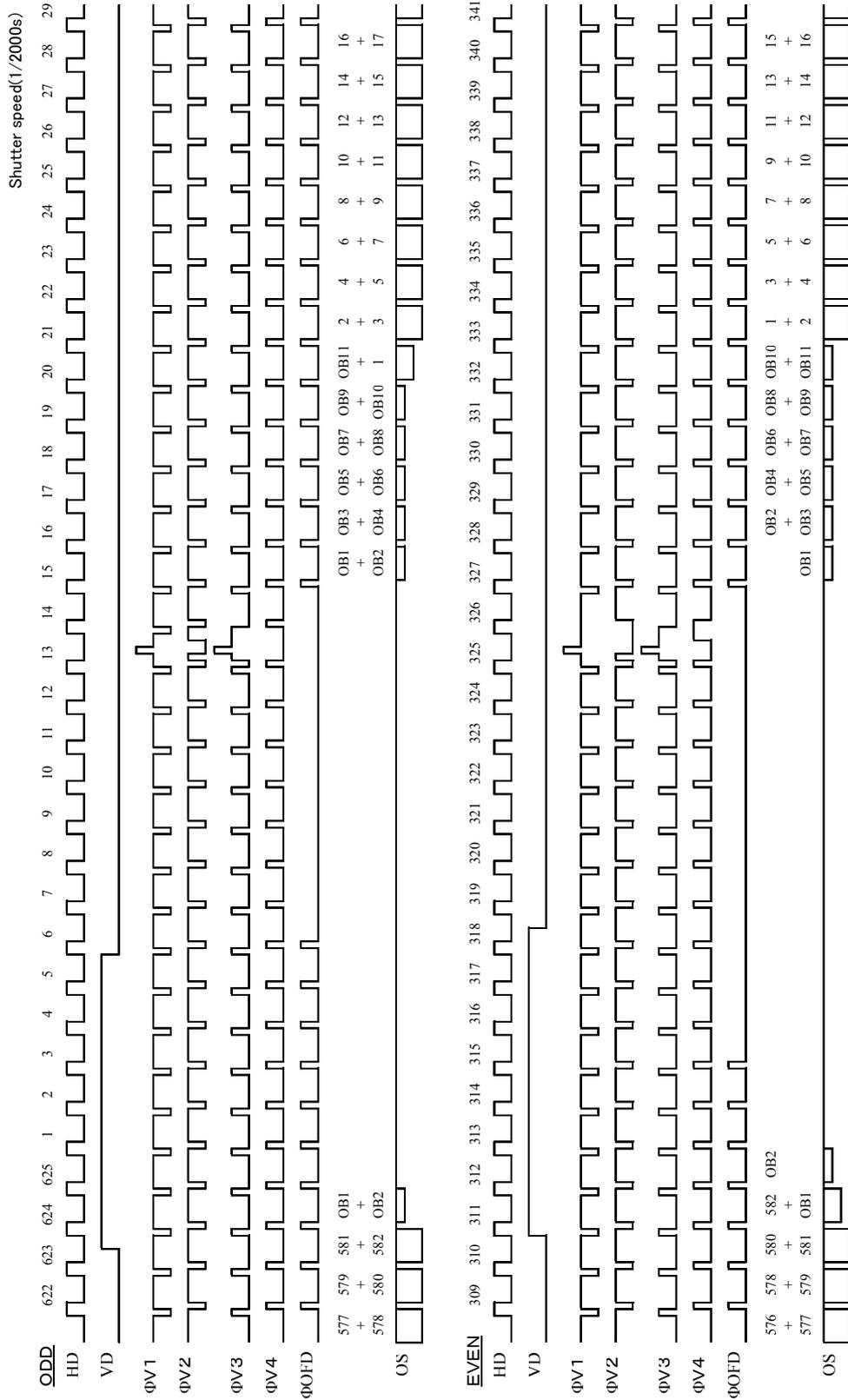
Note :

- (1) The average output voltage of under the uniform illumination. The standard exposure condition is defined when V_o is 150 mV.
- (2) The image area is divided into 10×10 segments under the standard exposure condition. The voltage of a segment is the average output voltage of all pixels within the segment. PRNU is defined by $(V_{max} - V_{min}) / V_o$, where V_{max} and V_{min} are the maximum and minimum values of each segment's voltage respectively.
- (3) The image area is divided into 10×10 segments. The segment's voltage is the average Output voltages of all pixels within the segment. V_{sat} is the minimum segment's voltage under 15 times exposure of the standard exposure condition.
- (4) The average output voltage under the non-exposure condition.
- (5) The image area is divided into 10×10 segments under the non-exposure condition. DSNU is defined by $(V_{dmax} - V_{dmin})$, where V_{dmax} and V_{dmin} are the maximum and minimum values of each segment's voltage respectively.
- (6) The average output voltage when a 1000 lux light source with a 90% reflector is imaged by a lens of F4, f50 mm.
- (7) The sensor is exposed only in the central area of $V/10$ square with a lens at F4, where V is the vertical image size. SMR is defined by the ratio of the output voltage detected during the vertical blanking period to the maximum of the output voltage in the $V/10$ square.
- (8) The sensor is exposed at the exposure level corresponding to the standard condition. AI is defined by the ratio between the output voltage measured at the 1st field during the non-exposure period and the standard output voltage.
- (9) The sensor is exposed only in the central area of $V/10$ square, where V is the vertical image size. ABL is the ratio between the exposure at the standard condition and the exposure at a point where a blooming is observed.
- (10) Observe with a vector scope when the color bar chart is imaged under the standard exposure condition.
- (11) The difference between the average output voltage of the (Mg+Ye),(G+Cy) line and the (Mg + Cy),(G + Ye) line under the standard exposure condition.
- (12) The difference between the average output voltage of the odd field and the even field

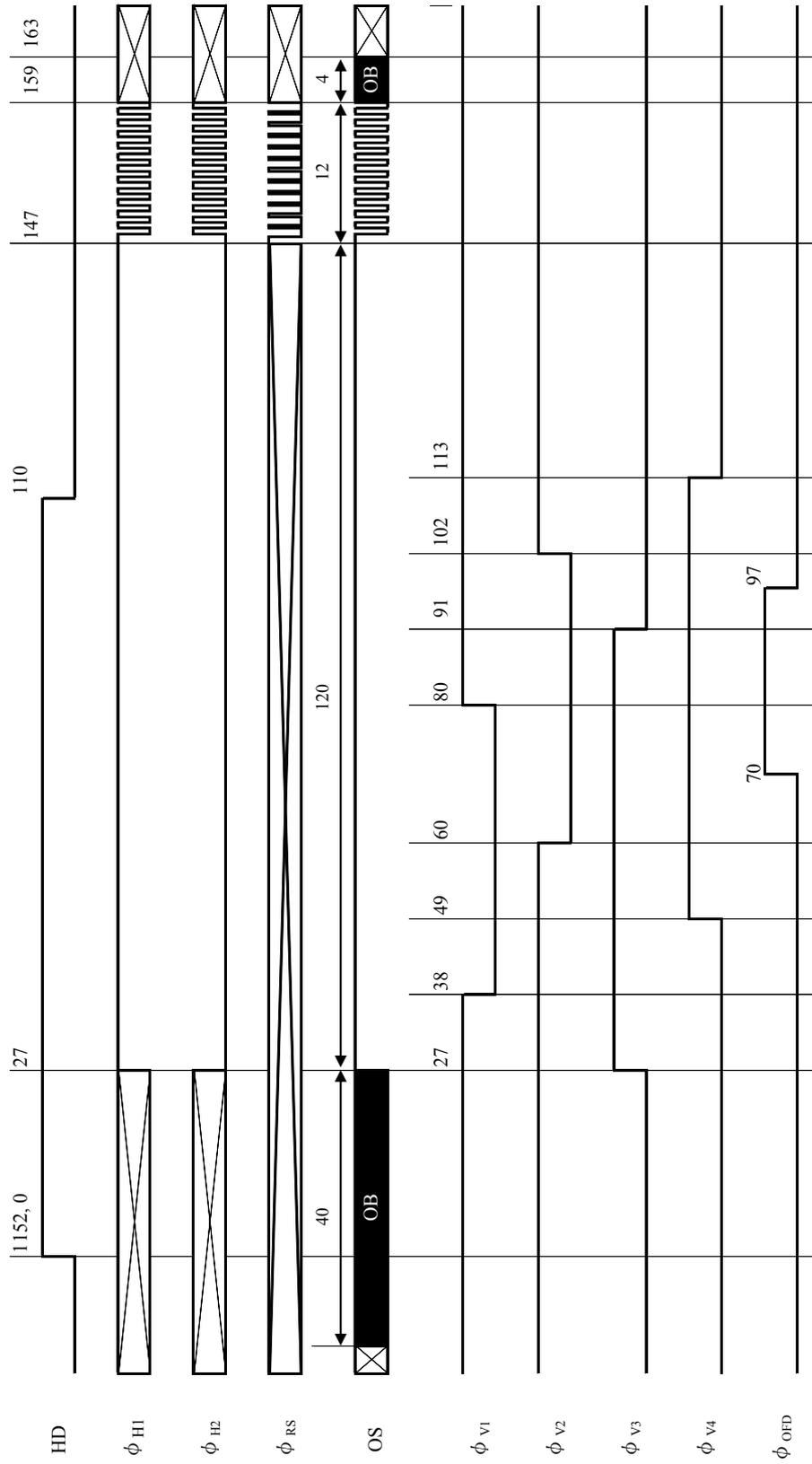
V_{OFD} of the internal output satisfies with ABL then 1000 times exposure of the standard exposure condition, and V_{sat} larger than 1200mV

7 DRIVE TIMING CHART EXAMPLE

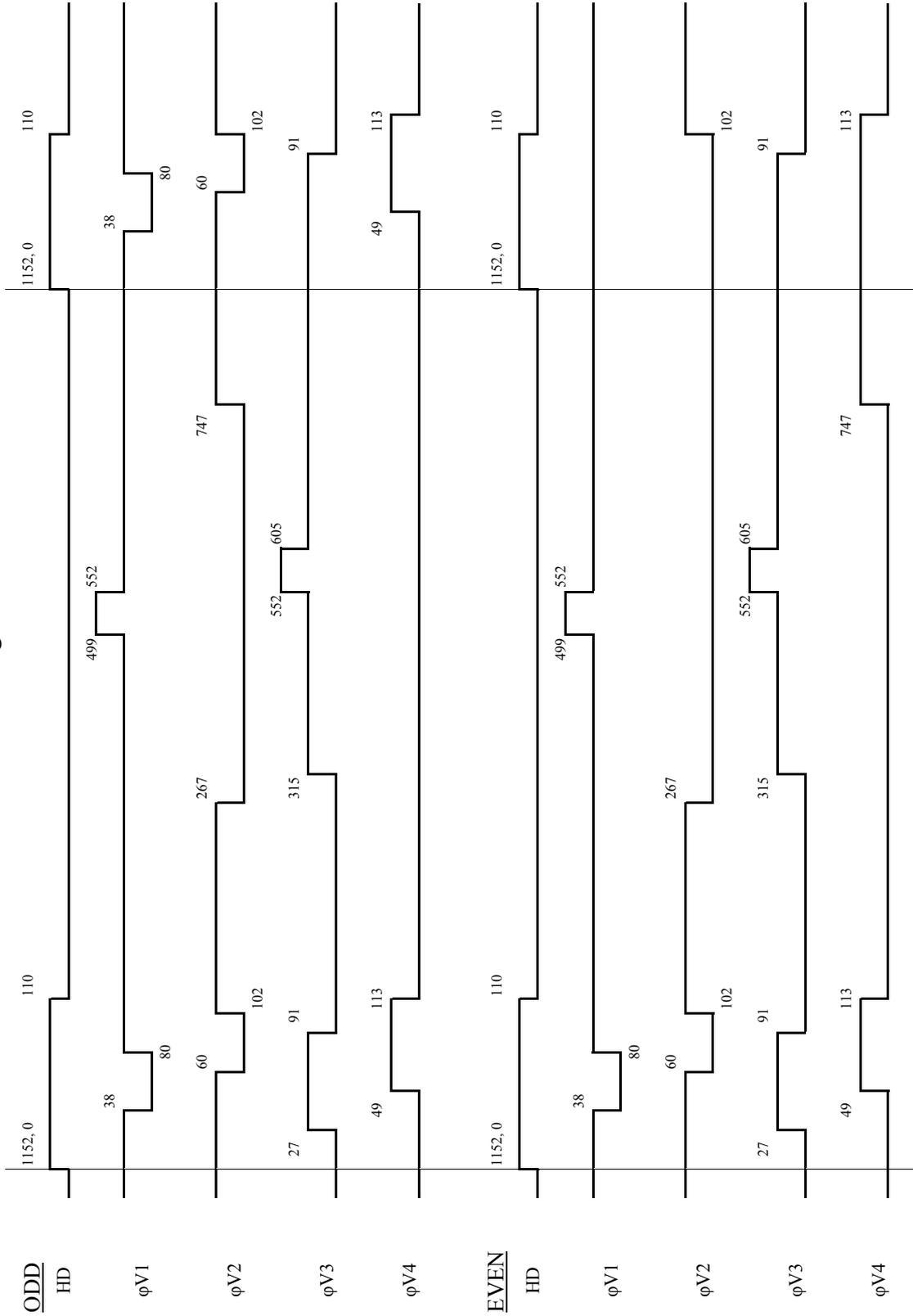
Vertical transfer timing



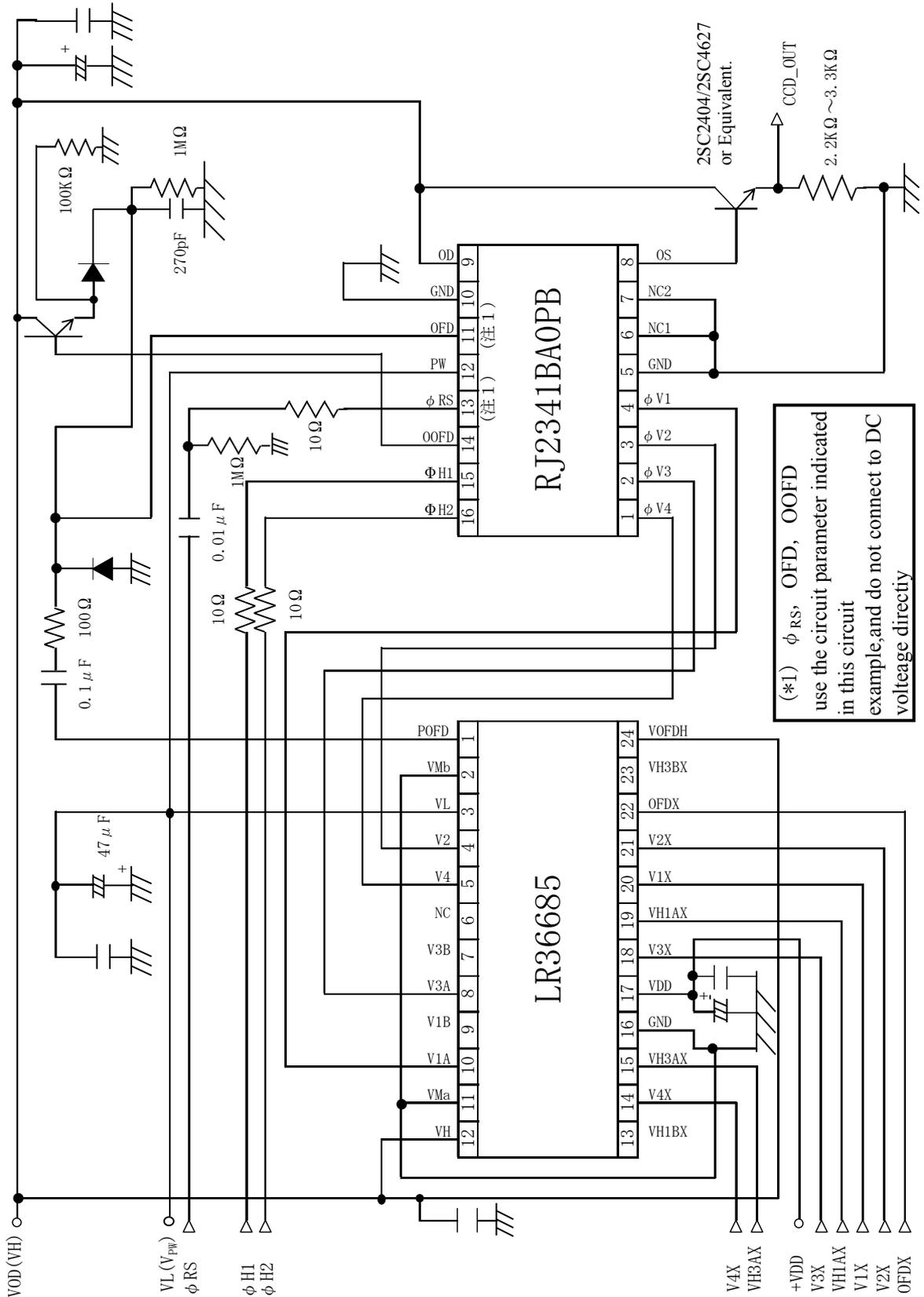
Horizontal transfer timing



Readout timing



8 EXAMPLE STANDARD OPERATING CIRCUIT



(*1) ϕ_{RS} , OFD, OOFD use the circuit parameter indicated in this circuit example, and do not connect to DC voltage directly

9 SPECIFICATIONS FOR BLEMISH

1 Definition of blemish

	Level of blemish (mV)	Permitted number of blemish		Comment
		AREA I	AREA II	
White blemish (Exposed)	$23 \leq B$	0		<ul style="list-style-type: none"> • See fig.9-1(a), fig.9-2 • $V_{out} = V_{std}$ • $M + N = 10$ Up to 4 blemishes are Allowed in AREA 1
	$13 \leq B < 23$	M		
	$B < 13$	no count		
Black blemish (Exposed)	$23 \leq B$	0		
	$13 \leq B < 23$	N		
	$B < 13$	no count		
White blemish (Non_exposed)		AREA I	AREA II	<ul style="list-style-type: none"> • See fig.9-1(b), fig.9-2 • Sum of the blemishes in AREA I and AREA II Are allowed up to 6.
	$12 < B$	0	0	
	$9 < B \leq 12$	1	3	
	$7 < B \leq 9$	2	4	
	$6 < B \leq 7$	4	5	
	$B \leq 6$	no count		
White blemish (Shutter mode)	$4.5 \leq B$	0		<ul style="list-style-type: none"> • See fig.9-1(a) • $V_{ou} = V_{std}/10$ • The electronic shutter Speed is set at 1/10000s
	$B < 4.5$	no count		
Black blemish (Shutter mode)	$4.5 \leq B$	0		
	$B < 4.5$	no count		

《Note》

- B : Blemish level defined in fig.9-1
- V_{out} : Average output voltage
- V_{std} : 150 mV. The standard output voltage defined in the specification of the characteristics.

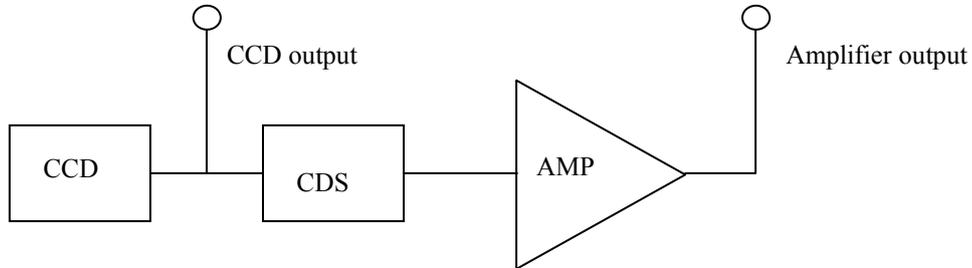
2) Definition of stain

The measuring area is divided into segments which include 20×20 pixels, respectively.

The difference between the average output voltage of neighboring segments is permitted below 1.5 mV, under the condition that the average output voltage of all imaging pixels is 75 mV (= $V_{std}/2$)

【MEASURING CONDITION】

- Ta : 60°C
- Measuring block diagram



The output voltage is measured at the CCD output.
 The gain of the amplifier is adjusted to the unity between the CCD output and the amplifier output.

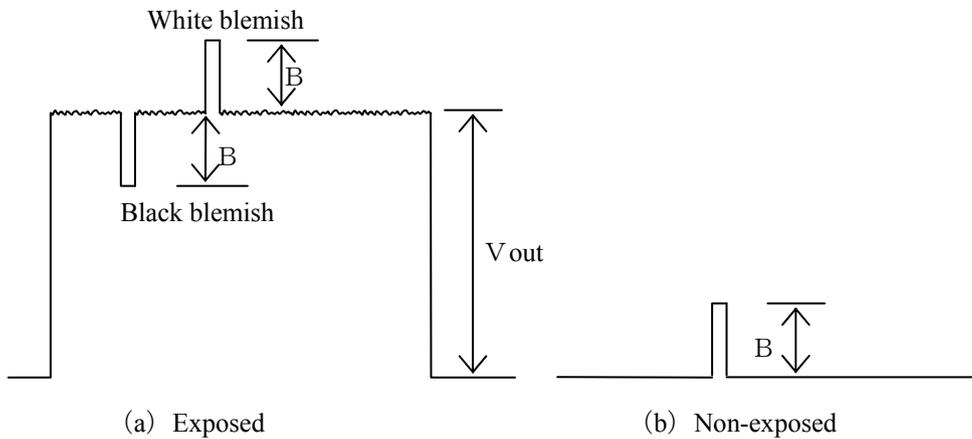


fig. 9-1 Definition of blemish level
 (The wave form is the luminance signal measured at the Amplifier output.)

【MEASURING AREA】

Measuring area includes all pixels in the image and the optical black area excluding the outer 10 pixels of the left and right sides and the outer 9 lines of the upper and lower sides in the image area.

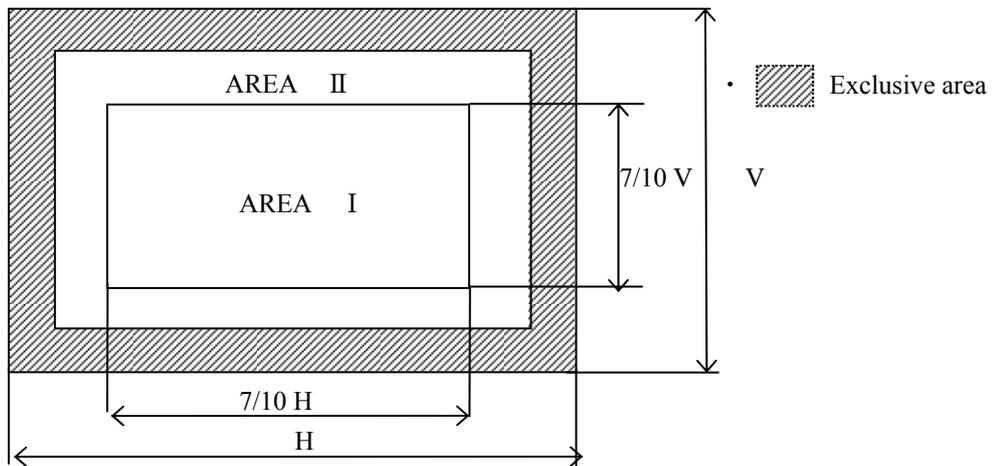


fig. 9-2 Definition of the measuring area

10 PRECAUTIONS

10.1. Package breakage

In order to prevent the package from being broken, observe the following instructions:

- 1) The CCD is a precise optical component and the package material is plastic.
Therefore,
 - Take care not to drop the device when mounting, handling, or transporting.
 - Avoid giving a shock to the package. Especially when leads are fixed to the socket and the circuit board, small shock could break the package more easily than when the package isn't fixed.

- 2) When mounting the package on the housing, be sure that the package is not bent.
If a bent package is forced into place between a hard plate or the like, the package may be broken.

- 3) If any damage or breakage occur on the surface of the glass cap, its characteristics could deteriorate.
Therefore,
 - Do not hit the glass cap.
 - Do not give a shock large enough to cause distortion.
 - Do not scrub or scratch the glass surface.Even a soft cloth or applicator, if dry, could cause dust to scratch the glass.

10.2. Electrostatic damage

As compared with general MOS-LSI, CCD has lower ESD.

Therefore, please take the following anti-static measures when handling the CCD:

- 1) Always discharge static electricity by grounding the human body and the instrument to be used.
To ground the human body, provide resistance of about 1 Meg ohm between the human body and the ground to be on the safe side.

- 2) When directly handling the device with fingers, hold the part without leads and do not touch any lead.

- 3) To avoid generating static electricity,
 - a. do not scrub the glass surface with cloth or plastic
 - b. do not attach any tape or labels
 - c. do not clean the glass surface with dust-cleaning tape

- 4) When storing or transporting the device, put it in a container of conductive material.

10.3. Dust and contamination

Dust or contamination on the glass surface could deteriorate the output characteristic or cause a scar. In order to minimize dust or contamination on the glass surface, take the following precautions:

- 1) Handle CCD in a clean environment such as a cleaned booth.
(The cleanliness level should be, if possible, class 1,000 at least.)
- 2) Do not touch the glass surface with fingers. If dust or contamination gets on the glass surface, the following cleaning method is recommended:
 - Dust from static electricity should be blown off with an ionized air blower. For anti-electrostatic measures, however, ground all the leads on the device before blowing off the dust.
 - The contamination on the glass surface should be wiped off with a clean applicator soaked in Isopropyl alcohol. Wipe slowly and gently in one direction only.Frequently replace the applicator and do not use the same applicator to clean more than one device.

※ Note: In most cases, dust and contamination are unavoidable, even before the device is first used. It is, therefore, recommended that the above procedures should be taken to wipe out dust and contamination before using the device.

10.4. Other

- 1) Soldering should be manually performed within 5 seconds at 350°C maximum at soldering iron.
- 2) Avoid using or storing the CCD at high temperature or high humidity as it is a precise optical component. Do not give a mechanical shock to the CCD.
- 3) As color filters are used in CCD, must not be exposed to strong light environment such as UV and direct sun light for long periods during your use, storage, transportation and fabrication. If exposed to strong light environment for long periods, color filters will be discolored. When strong light is radiated to CCD, CCD image could be persisted even without bias.
- 4) The color filters of this CCD are fabricated of pigment color filter materials which have better light resistance performance. When it is used in surveillance camera, however, CCD image could be persisted if it captures light source for long periods even if it is indoor light (fluorescent lamp, incandescent lamp, etc.) or outdoor light (fluorescent lamp, mercury lamp, etc.). This phenomenon could happen at power-off when fixed iris lens is used.
- 5) The color filters of this CCD are fabricated of pigment color filter materials which have better light resistance performance. When it is used for capturing high luminance object by electronic iris exposure control system, however, object luminance may become excessive and it will possibly accelerate the discoloration of its color filter. In such a case, it is advisable that taking lens with the automatic iris and closing of the shutter during the power-off mode should be properly arranged. Prior to using this CCD continuously in a severe environment which exceeds normal conditions, consult our company.
- 6) The exit pupil position of lens should be more than 25 mm from the top surface of the CCD.
- 7) CCD has the possibility that white blemish, which originates in the structure of CCD with the passage of time by an external factor such as the radiations, could be generated. Please use white blemish compensation circuit for white blemish generated afterward.

11 PACKAGE OUTLINE AND PACKING SPECIFICATION

11. 1 Package Outline Specification

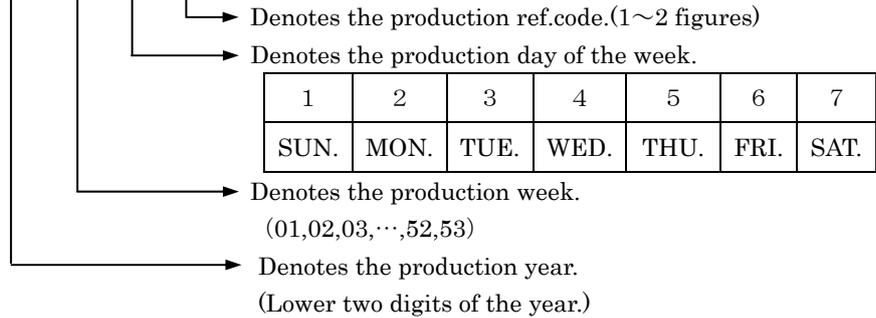
Refer to attached drawing.

(The seal resin stick out from the package shall be passed. And, the seal resins are two kinds of colors, white and transparency.)

11. 2 Markings

Marking contents

- (1). Product name : R J 2 3 4 1 B A 0 P B
- (2). Company name : S H A R P
- (3). Country of origin : J A P A N
- (4). Date code : Y Y W W X X X



Positions of markings are shown in the package outline drawing.

But, markings shown in that drawing are not provided any measurements of their characters and their positions.

11. 3 Packing Specification

3 - 1. Packing materials

Material Name	Material Spec.	Purpose
Device case	Cardboard(300devices/case)	Device tray fixing
Device tray	Conductive plastic (50devices/tray)	Device packing(6trays/case)
Cover tray	Conductive plastic(1tray/case)	Device packing
PP band	Polypropylene	Device tray fixing
Buffer	Cardboard(2sheets/case)	Shock absorber of device tray
Plastic film bag	Plastic film	Device tray fixing
Tape	Paper	Sealing plastic film bag and device case
Label	Paper	Indicates part number, quantity and date of manufacture

3 - 2. External appearance of packing

Refer to attached drawing

11. 4 Precaution

- 1). Before unpacking, confirm the imports of the chapter "Handling Precaution" in this device specification.
- 2). Unpacking should be done on the stand treated with anti-ESD. At that time, the same anti-ESD treatment should be done to operator's body, too.

ISSUE NUMBER	(NOTE)
2 5 2 5 2 A D C	

11. 5 Chemical substance information in the product

Product Information Notification based on Chinese law, Management Methods for Controlling Pollution by Electronic Information Products.

Names and Contents of the Toxic and Hazardous Substances or Elements in the Product

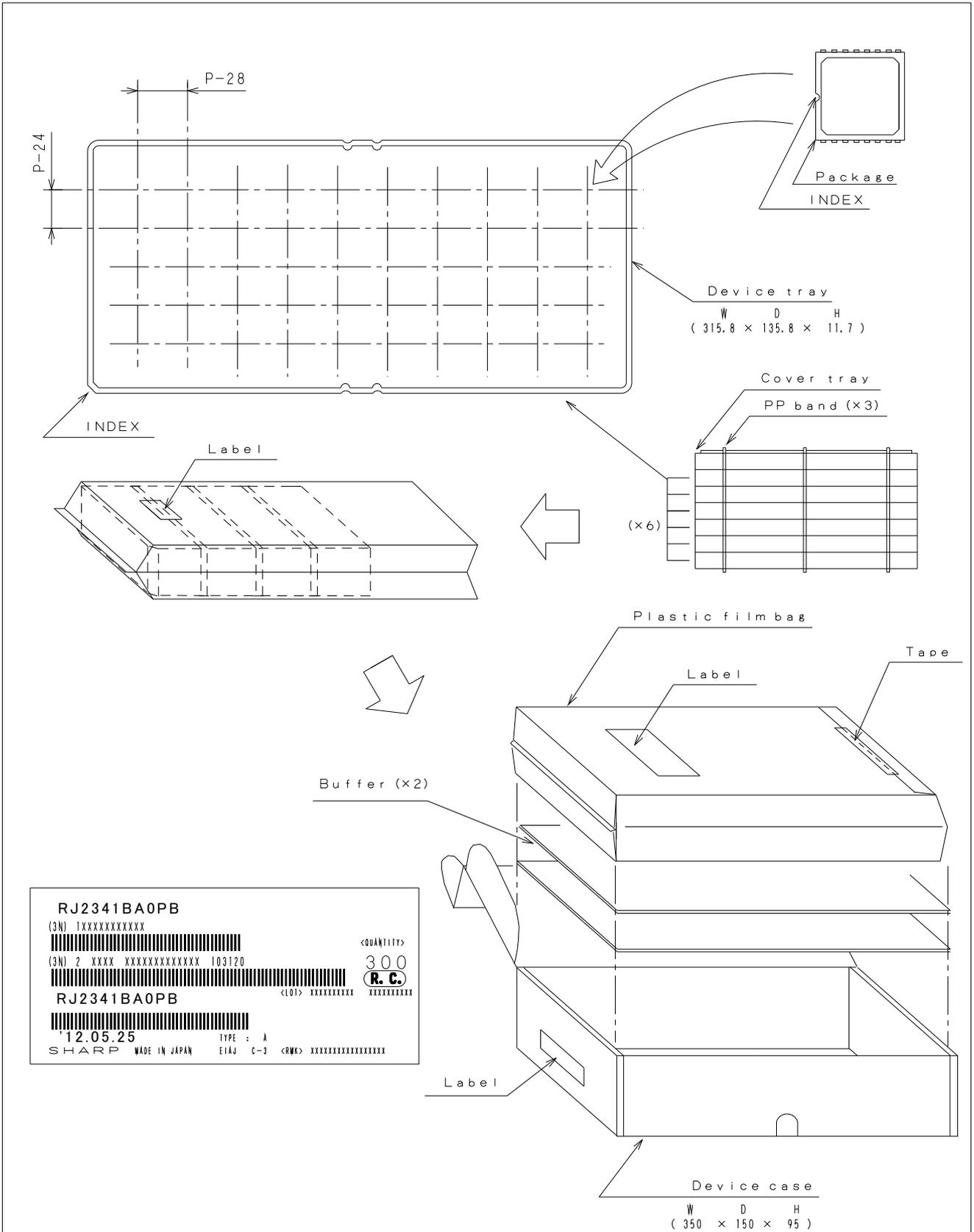
Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
○	○	○	○	○	○

○ : indicates that the content of the toxic and hazardous substance in all the homogeneous materials of the part is below the concentration limit requirement as described in SJ/T 11363-2006.

× : indicates that the content of the toxic and hazardous substance in at least one homogeneous material of the part exceeds the concentration limit requirement as described in SJ/T 11363-2006 standard.

ISSUE NUMBER

2 5 2 5 2 A D C



RJ2341BA0PB

(3N) 1XXXXXXXXXX

(3N) 2 XXXX XXXXXXXXXXXXXXX 103120

RJ2341BA0PB

12.05.25

SHARP MADE IN JAPAN

TYPE : A

EIAJ C-3

<QUANTITY> 300

<LOT> XXXXXXXX XXXXXXXX

R.C.

<RMK> XXXXXXXXXXXXXXX

(UNIT : mm)

材質 MATERIAL	仕上 FINISH	名称 NAME	External Appearance of Packing			
Assembly Process Technology Development Dept		コード CODE				
ELECTRONIC COMPONENTS AND DEVICES GROUP		図番 DRAWING No.	K S E C -3 0 0 T A -C			
SHARP CORPORATION						