SHARP

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To : _____

PRELIMINARY

SPECIFICATIONS

Product Type 1/3-type Progressive Scan B/W CCD Area Sensor with 1320k Pixels

Model No R J 3 3 J 4 C A 0 D T

※ This specifications contains 32 pages including the cover and appendix.
If you have any objections, please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

DATE : _____

BY : _____

PRESENTED

BY : J. Nakai

J.NAKAI
Dept. General Manager

SHARP CORPORATION
SENSING DEVICE DIVISION DEV. DEPT. V
Jul 17 2015
MAIL DATE
ELECTRONIC COMPONENTS AND DEVICES GROUP

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SHARP CORPORATION

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(2) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (3), even for the following application areas, be sure to observe the precautions given in Paragraph (3). Never use the products for the equipment listed in Paragraph (4).
Office electronics
- Instrumentation and measuring equipment
- Machine tools
- Audiovisual equipment
- Home appliance
- Communication equipment other than for trunk lines

(3) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.
- Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
- Mainframe computers
- Traffic control systems
- Gas leak detectors and automatic cutoff devices
- Rescue and security equipment
- Other safety devices and safety equipment, etc

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- Aerospace equipment
- Communications equipment for trunk lines
- Control equipment for the nuclear power industry
- Medical equipment related to life support, etc.

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○ Please direct all queries and regarding the products covered herein to a sales representative of the company.

CONTENTS

RJ33J4CA0DT

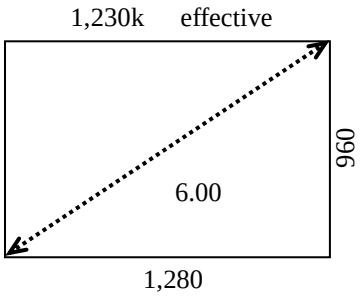
1/3-type Progressive Scan B/W CCD Area Sensor with 1320k Pixels

1 DESCRIPTION

The RJ33J4CA0DT is a 1/3-type solid-state image sensor that consists of PN photo-diodes and CCDs（charge-coupled devices）. With approximately 1,320k pixels, the sensor provides a high resolution stable B/W image.

1 . 1 Features

1）Optical size : 6.00 mm（Aspect ratio 4：3）
2）Progressive scan format
3）Square pixel
4）Number of total pixels : Horizontal 1372 ×Vertical 986
Number of image pixels : Horizontal 1320 ×Vertical 976
Number of effective pixels : Horizontal 1280 ×Vertical 960
Pixel pitch : Horizontal 3.75 μ m ×Vertical 3.75 μ m
Number of optical black pixels : Horizontal ; 12 front and 40 rear
: Vertical ; 8 front and2 rear
Number of dummy bits : Horizontal ; 4, Vertical ; 2
5）B/W image
6）Supports monitoring mode
7）Built-in overflow drain voltage output circuit, and reset gate voltage circuit
8）Variable electronic shutter
9）Low fixed pattern noise and lag
10）No burn-in and no image distortion
11）Blooming suppression structure
12）Built-in output amplifier
13）N-type silicon substrate, N-MOS process,
Not designed or rated as radiation hardened
14）Global shutter



1 . 2 Applications

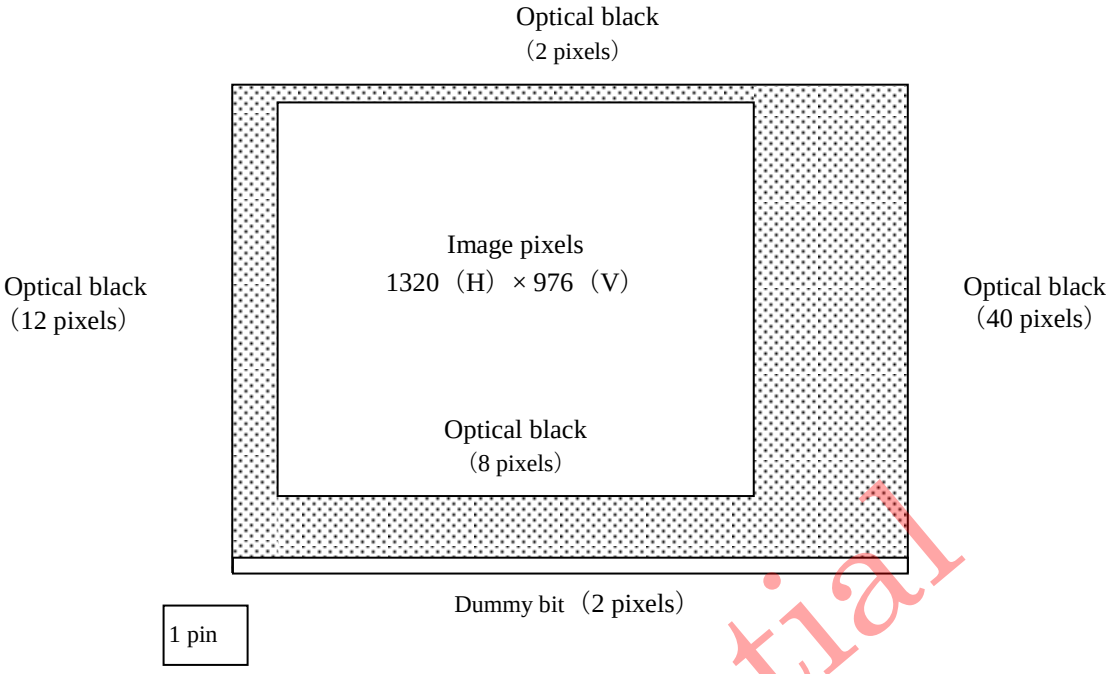
1）Cameras (Security cameras, Camcorders, Industrial monitor cameras, etc.)
2）Pattern recognition

iSHCCD Ⅱ in iSHartina

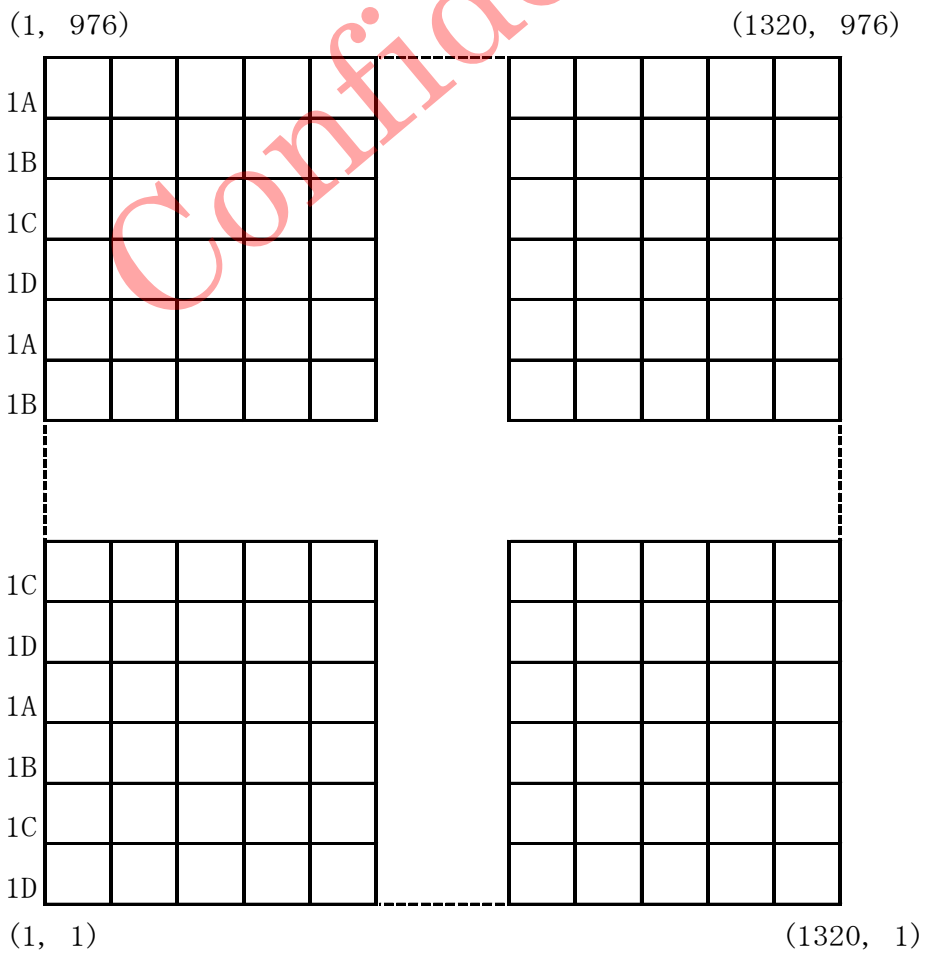
"iSHCCD Ⅱ", "iSHCCD" and "iSHartina" are the trademarks of Sharp Corporation.
The "iSHCCD Ⅱ" is an advanced CCD image sensor that drastically improves light efficiency by including near-infrared light region as a basic structure of "iSHCCD".
The "iSHartina" series is a key device group of Sharp which realizes a next-generation sensing world.

The circuit diagram and others included in this specifications are intended for use to explain typical application examples. Therefore, we take no responsibility for any problem as may occur due to the use of the included circuit and for any problem with industrial proprietary rights or other rights.

2 ARRANGEMENT OF PIXELS

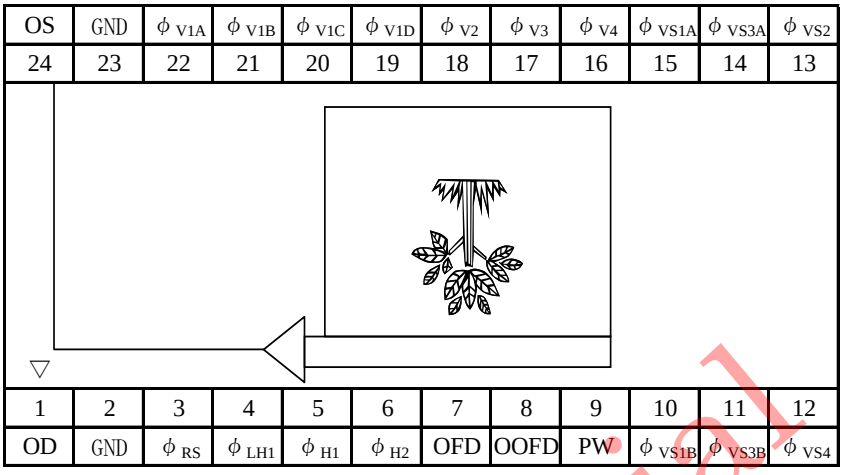


Pin arrangement of the vertical readout clock



3 PIN CONFIGURATION（TOP VIEW）

・EXAMPLE OF PIN CONFIGURATION FOR THE STANDARD OPERATING CIRCUIT -1
（When the number of ϕ V terminals is 13, please connect in this example of a circuit.-1）



Symbol	Pin name
OD	Output transistor drain
OS	Output signals
ϕ RS	Reset transistor clock
ϕ V1A, ϕ V1B, ϕ V1C, ϕ V1D, ϕ V2, ϕ V3, ϕ V4, ϕ VS1A ϕ VS1B, ϕ VS2, ϕ VS3A, ϕ VS3B, ϕ VS4	Vertical shift register clock
ϕ LH1, ϕ H1, ϕ H2	Horizontal shift register clock
OFD	Overflow drain
OOFD	Output overflow drain
PW	P_well
GND	Ground

In addition, ϕ V terminals are reducible like the following cases.

[ϕ V terminals ＝ 13 → 12 or, 8]

・EXAMPLE OF PIN CONFIGURATION FOR THE OPERATING CIRCUIT -2

（When the number of ϕ V terminals is 12, please connect in this example of a circuit.-2）

[Please use it, connecting ϕv3=ϕvS3A]

OS	GND	ϕ_{V1A}	ϕ_{V1B}	ϕ_{V1C}	ϕ_{V1D}	ϕ_{V2}	ϕ_{V3}	ϕ_{V4}	ϕ_{VS1A}	(= ϕ_{V3})	ϕ_{VS2}
24	23	22	21	20	19	18	17	16	15	14	13
1	2	3	4	5	6	7	8	9	10	11	12
OD	GND	ϕ_{RS}	ϕ_{LH1}	ϕ_{H1}	ϕ_{H2}	OFD	OOFD	PW	ϕ_{VS1B}	ϕ_{VS3B}	ϕ_{VS4}

・EXAMPLE OF PIN CONFIGURATION FOR THE OPERATING CIRCUIT -3

（When the number of ϕ V terminals is 8, please connect in this example of a circuit.-3

However, 4-pixels addition[VGA]60 frames/s -mode cannot be used in the example of the circuit-3.）

[Please use it, connecting ϕv1A = ϕv1B、ϕv1C = ϕv1D、ϕv2 = ϕvS2、ϕvS1A= ϕvS1B、ϕvS3A= ϕvS3B]

OS	GND	ϕ_{V1A}	(= ϕ_{V1A})	ϕ_{V1C}	(= ϕ_{V1C})	ϕ_{V2}	ϕ_{V3}	ϕ_{V4}	ϕ_{VS1A}	ϕ_{VS3A}	(= ϕ_{V2})
24	23	22	21	20	19	18	17	16	15	14	13
1	2	3	4	5	6	7	8	9	10	11	12
OD	GND	ϕ_{RS}	ϕ_{LH1}	ϕ_{H1}	ϕ_{H2}	OFD	OOFD	PW	(= ϕ_{VS1A})	(= ϕ_{VS3A})	ϕ_{VS4}

4 ABSOLUTE MAXIMUM RATINGS

(T_A=25℃)

Parameter	Symbol	Ratings	Unit
Output transistor drain voltage	V_{OD}	0 to +15.4	V
Overflow drain voltage	V_{OFD}	0 to +32	V
Overflow drain output voltage	V_{OOFD}	Internal output（Note 1）	
Reset gate clock voltage	$V_{\phi RS}$	Internal output（Note 2）	
Vertical shift register clock voltage	$V_{\phi V}$	V_{PW} to +15.4	V
Horizontal shift register clock voltage	$V_{\phi H}$	-0.3 to +5.1	V
Voltage difference between P_well and vertical clock	V_{PW}-$V_{\phi V}$	-23.8 to +0	V
Voltage difference between vertical clocks	$V_{\phi V}$-$V_{\phi V}$	0 to +9.9（Note 3）	V
Storage temperature	T_{STG}	-40 to +90	℃
Ambient operating temperature	T_{OPR}	-30 to +85	℃

(Note 1) Use the circuit parameter indicated in “EXAMPLE OF STANDARD OPERATING CIRCUIT” and do not connect to DC voltage directly. When OOFD is connected to GND, connect V_{OD} to GND.

(Note 2) Do not connect to DC voltage directly. When ϕ_{RS} is connected to GND, connect V_{OD} to GND.Reset gate clock is applied below 5.1 Vp-p.

(Note 3) When clock width is below 10 μs, and clock duty factor is below 0.1 %, voltage differencebetween adjoining vertical clocks are guaranteed up to 15.4 V.

Do not change all ϕ_V during 0.5 μs before rising edge of $V_{\phi VH}$ pulse and after falling edge of $V_{\phi VH}$ pulse.

Do not change directly into $V_{\phi VL}$→$V_{\phi VH}$ or $V_{\phi VH}$→$V_{\phi VL}$.

5 RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min.	Typ.	Max.	Unit
Ambient operating temperature		T_{OPR}		25.0		℃
Output transistor drain voltage		V_{OD}	13.1	13.5	13.9	V
Overflow drain clock	p-p level（Note 1）	$V_{\phi OFD}$	19.3	20.0	20.7	V
Ground		GND		0.0		V
P_well voltage	（Note 2）	V_{PW}	-6.8		$V_{\phi VL}$	V
Vertical shift register clock	LOW level	$V_{\phi V1AL}$, $V_{\phi V1BL}$, $V_{\phi V1CL}$, $V_{\phi V1DL}$, $V_{\phi V2L}$, $V_{\phi V3L}$, $V_{\phi V4L}$, $V_{\phi VS1AL}$, $V_{\phi VS1BL}$, $V_{\phi VS2L}$, $V_{\phi VS3AL}$, $V_{\phi VS3BL}$, $V_{\phi VS4L}$	-6.8	-6.5	-6.2	V
	INTERMEDIATE level	$V_{\phi V1AI}$, $V_{\phi V1BI}$, $V_{\phi V1CI}$, $V_{\phi V1DI}$, $V_{\phi V2I}$, $V_{\phi V3I}$, $V_{\phi V4I}$, $V_{\phi VS1AI}$, $V_{\phi VS1BI}$, $V_{\phi VS2I}$, $V_{\phi VS3AI}$, $V_{\phi VS3BI}$, $V_{\phi VS4I}$		0.0		V
	HIGH level	$V_{\phi V1AH}$, $V_{\phi V1BH}$, $V_{\phi V1CH}$, $V_{\phi V1DH}$	13.1	13.5	13.9	V
Horizontal shift register clock	LOW level	$V_{\phi H1L}$, $V_{\phi H2L}$, $V_{\phi LH1L}$	-0.05	0.0	0.05	V
	HIGH level	$V_{\phi H1H}$, $V_{\phi H2H}$, $V_{\phi LH1H}$	3.15		3.6	V
Reset gate clock	p-p level（Note 1）	$V_{\phi RS}$	3.15		3.6	V
Vertical shift register clock frequency （Note 3）		$f_{\phi V1A}$,$f_{\phi V1B}$, $f_{\phi V1C}$,$f_{\phi V1D}$, $f_{\phi V2}$,$f_{\phi V3}$,$f_{\phi V4}$, $f_{\phi VS1A}$,$f_{\phi VS1B}$, $f_{\phi VS2}$,$f_{\phi VS3A}$, $f_{\phi VS3B}$,$f_{\phi VS4}$		29.8		kHz
Horizontal shift register clock frequency		f_{H1},f_{H2},f_{LH1}		45.0		MHz
Reset gate clock frequency		$f_{\phi RS}$		45.0		MHz

（Note 1） Use the circuit parameter indicated in “EXAMPLE OF STANDARD OPERATING CIRCUIT”, and do not connect to DC voltage directly.

（Note 2） V_{PW} is set below $V_{\phi VL}$ that is low level of vertical shift register clock, or is used with the same power supply that is connected to V_L of V driver IC.

（Note 3） At frame accumulation mode.

※ To apply power, first connect GND and then turn on V_{OD}. After turning on V_{OD}, turn on V_{PW} first and then turn on other powers and pulses.
Do not connect the device to or disconnect it from the plug socket while power is being applied.

6 CHARACTERISTICS（Drive method：1/30s frame accumulation）

T_A：+25℃, but +60℃ for parameter No.4 and No.5.
Operating conditions：the typical values specified in “5 RECOMMENDED OPERATING CONDITIONS”.
Color temperature of light source：3200K, IR cut-off filter（CM-500,1 mmt）is used.

No.	Parameter	Symbol	Note	Min.	Typ.	Max.	Unit
1	Standard output voltage	V_O	1		150		mV
2	Photo response non-uniformity	PRNU	2			10	%
3	Saturation output voltage	V_{SAT}	3	700			mV
4	Dark output voltage	V_{DARK}	4		0.5	3.0	mV
5	Dark signal non-uniformity	DSNU	5		0.5	2.0	mV
6	Sensitivity	R	6	1140	1430		mV
7	Smear ratio	SMR	7		-120	-100	dB
8	Image lag	AI	8			1.0	%
9	Blooming suppression ratio	ABL	9	1000			
10	Output transistor drain current	I_{OD}			6.0	9.0	mA

【 Notes 】

1 The average output voltage of signal under the uniform illumination. The standard exposure conditions are defined as when V_O is 150 mV.
2 The image area is divided into 10 × 10 segments under the standard exposure conditions. Each segment’s voltage is the average output voltage of all pixels within the segment. PRNU is defined by （Vmax - Vmin） / V_O, where Vmax and Vmin are the maximum and minimum values of each segment’s voltage respectively.
3 The image area is divided into 10 × 10 segments. Each segment’s voltage is the average output voltages of all pixels within the segment. V_{SAT} is the minimum segment’s voltage under 10 times exposure of the standard exposure conditions.
4 The average output voltage under non-exposure conditions.
5 The image area is divided into 10 × 10 segments under non-exposure conditions. DSNU is defined by（Vdmax – Vdmin）, where Vdmax and Vdmin are the maximum and minimum values of each segment’s voltage respectively.
6 The average output voltage of signal when a 1000 lux light source with a 90 % reflector is imaged by a lens of F4, f50 mm.
7 The sensor is exposed only in the central area of V/10 square with a lens at F4, where V is the vertical image size. SMR is defined by the ratio of the output voltage detected during the vertical blanking period to the maximum output voltage in the V/10 square.
8 The sensor is exposed at the exposure level corresponding to the standard conditions. AI is defined by the ratio of the output voltage measured at the 1st field during the non-exposure period to the standard output voltage.
9 The sensor is exposed only in the central area of V/10 square, where V is the vertical image size. ABL is defined by the ratio of the exposure at the standard conditions to the exposure at a point where blooming is observed.

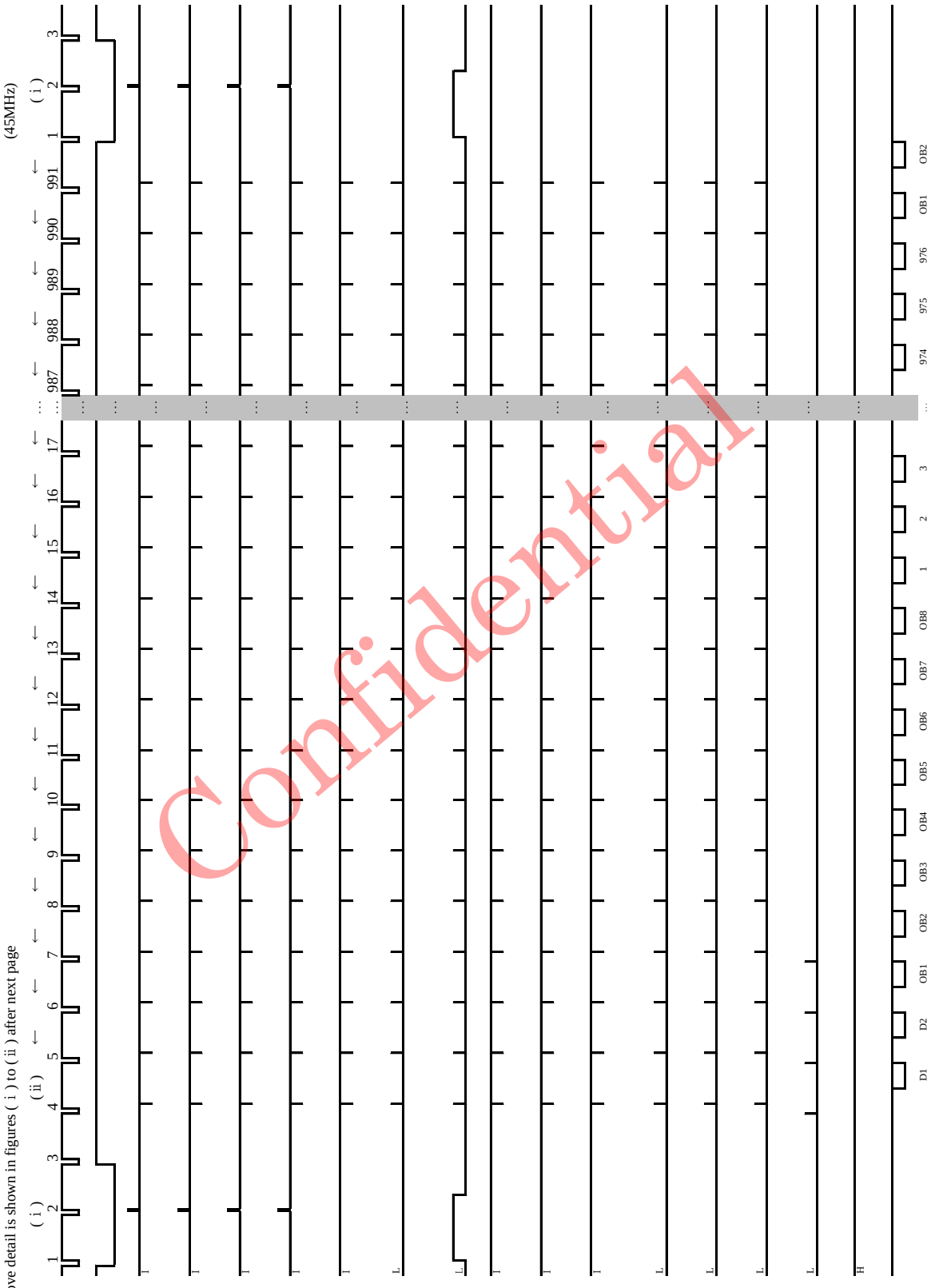
【 Comment 】

Within the recommended operating conditions of V_{OD}, V_{OFD} of the internal output satisfies with ABL and V_{SAT}.

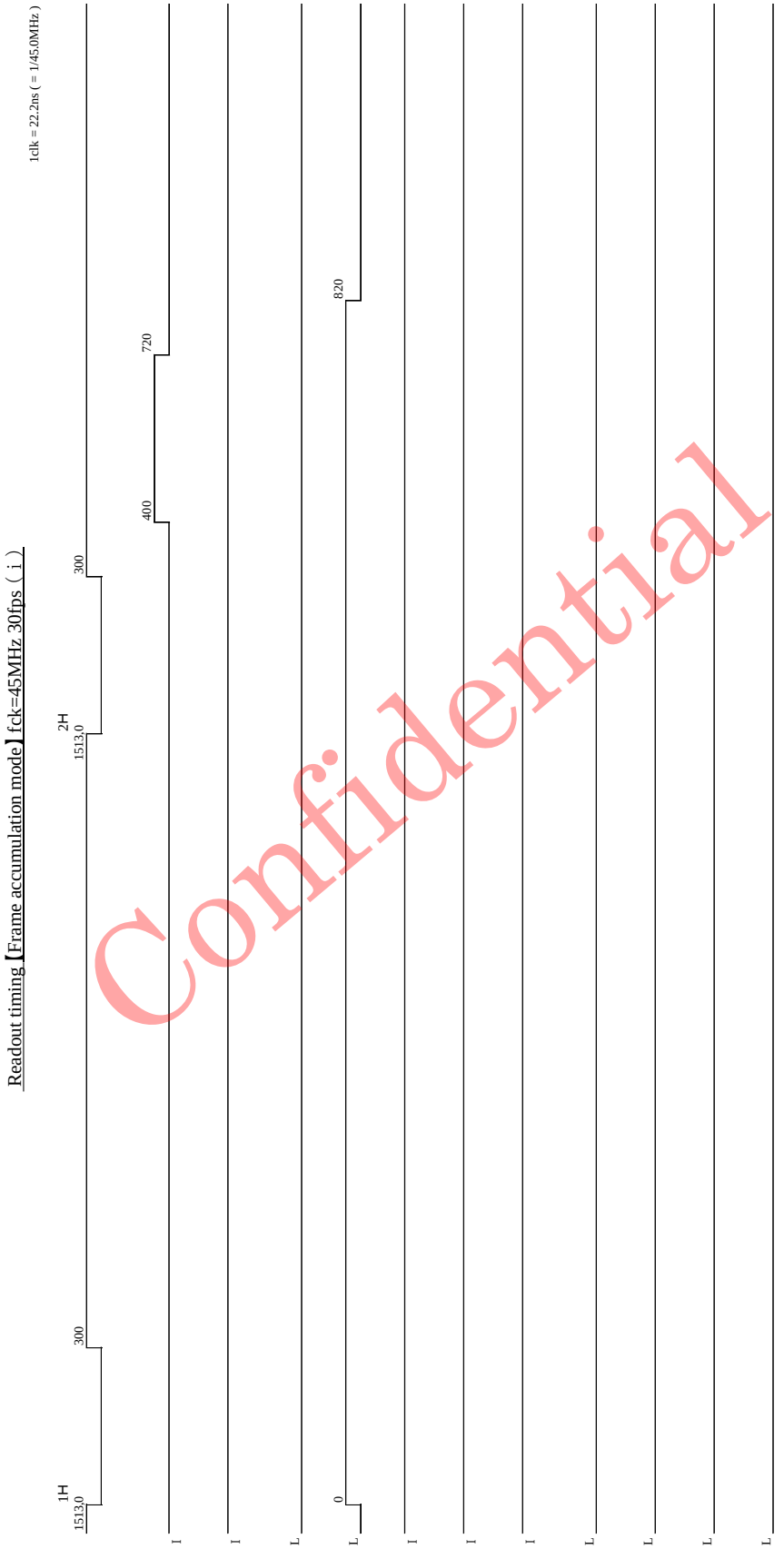
7 DRIVE TIMING CHART

Vertical transfer timing【Frame accumulation mode】fck=45MHz 30fps

Pulse diagram in move detail is shown in figures (i) to (ii) after next page

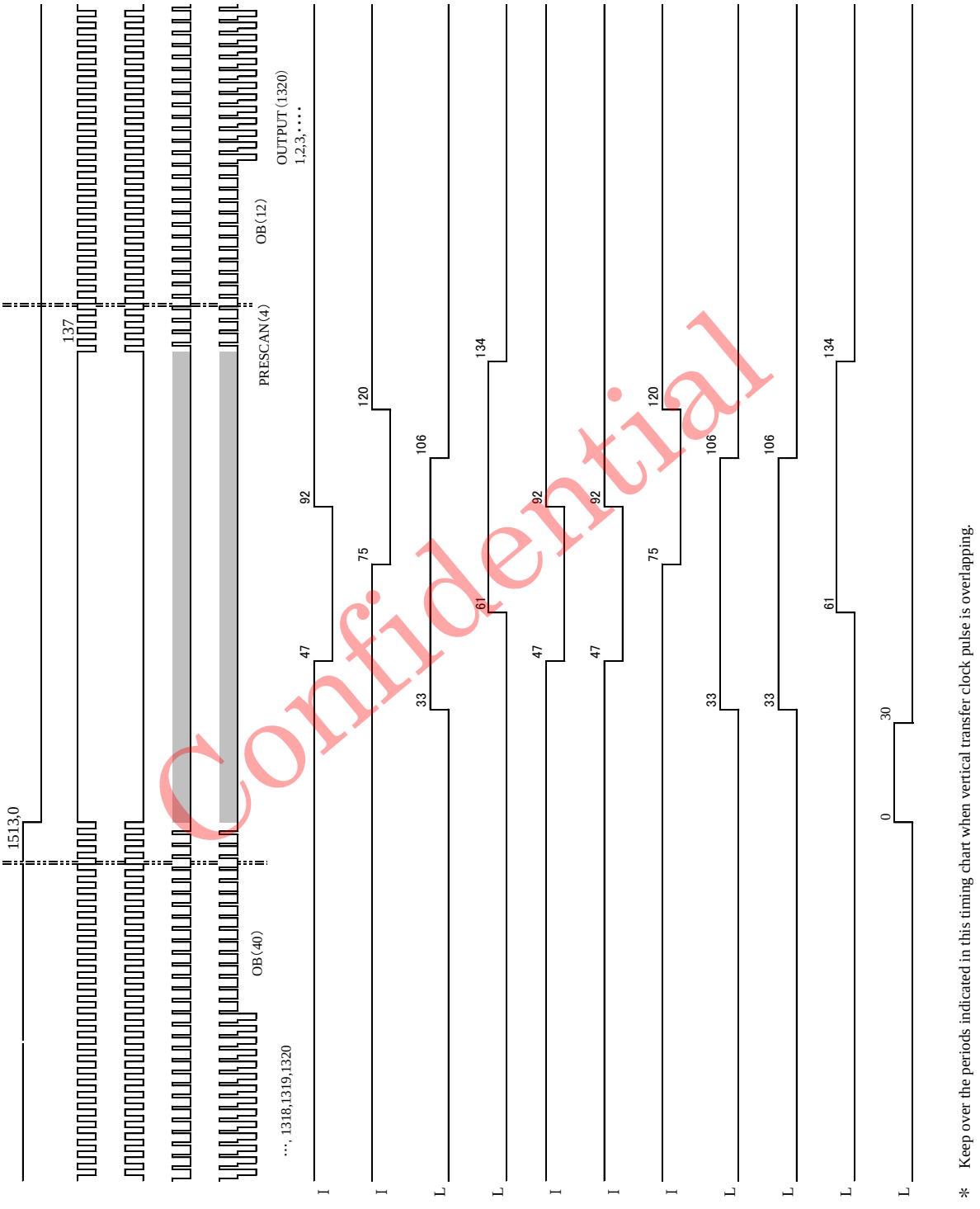


Readout timing【Frame accumulation mode】fck=45MHz 30fps (i)



* Keep over the periods indicated in this timing chart when vertical transfer clock pulse is overlapping.

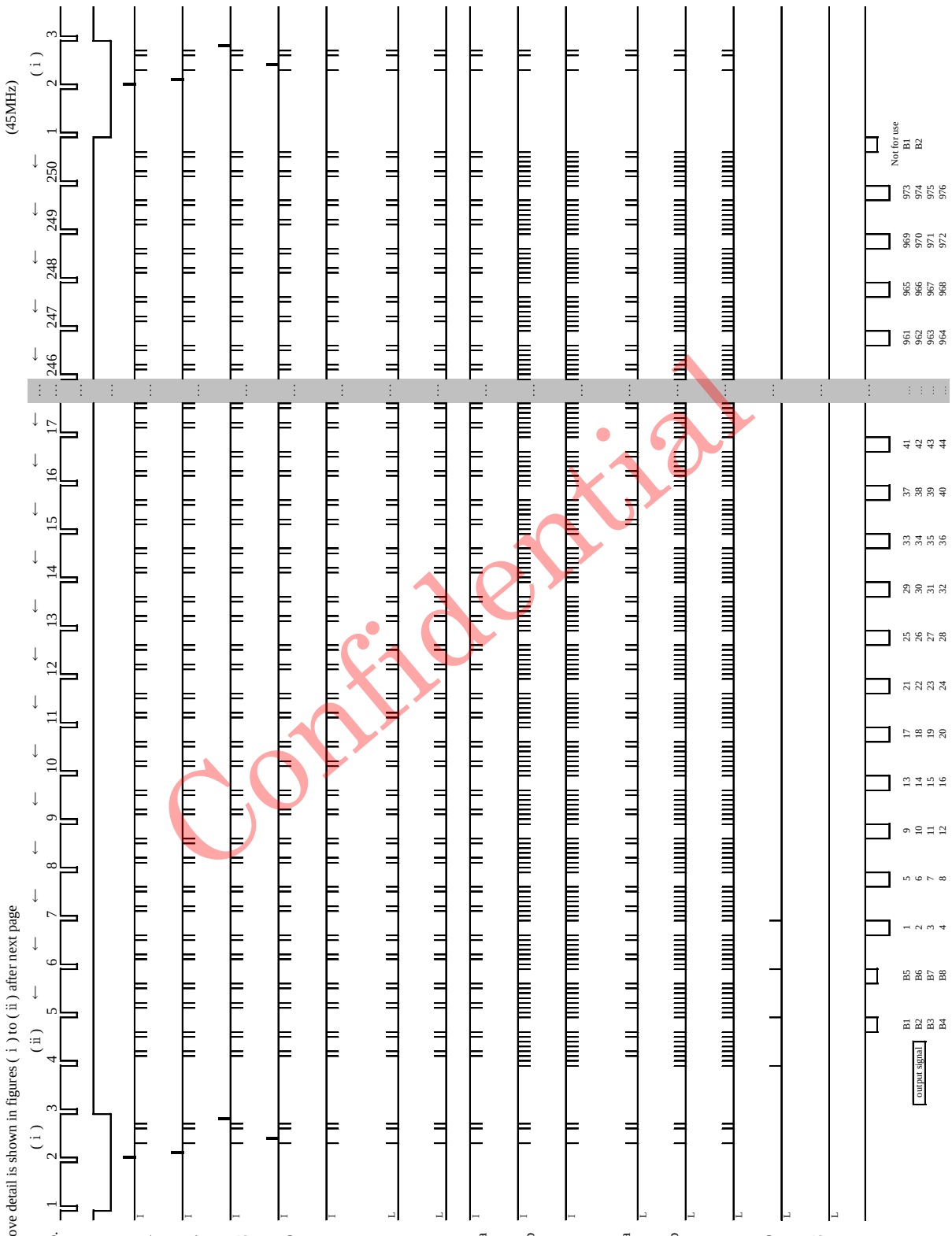
Horizontal transfer timing【Frame accumulation mode】fck=45MHz 30fps（ii）



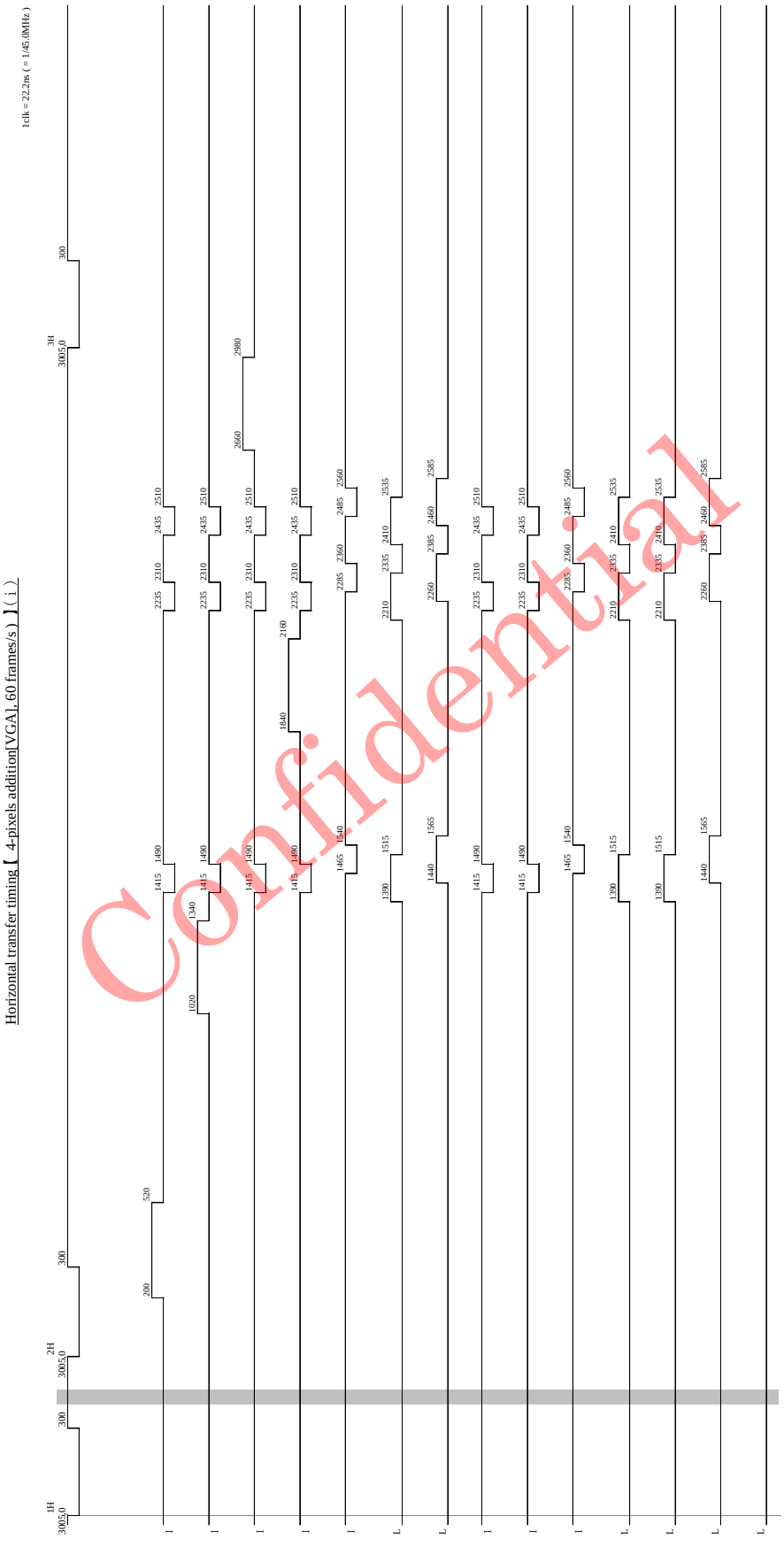
* Keep over the periods indicated in this timing chart when vertical transfer clock pulse is overlapping.

Vertical transfer timing 【 4-pixels addition[VGA], 60 frames/s) 】

Pulse diagram in move detail is shown in figures (i) to (ii) after next page

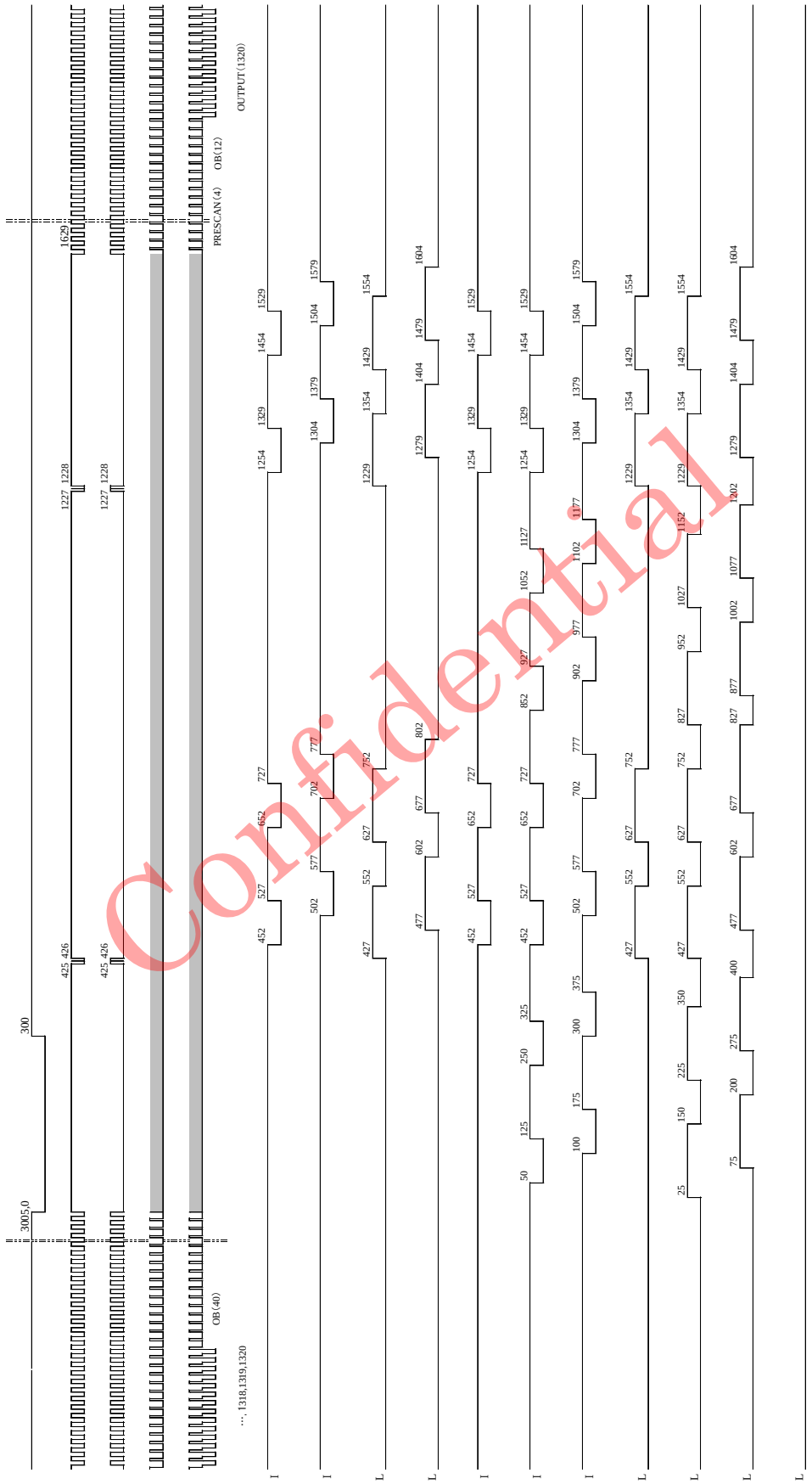


Horizontal transfer timing【 4-pixels addition[VGA], 60 frames/s 】(i)



* Keep over the periods indicated in this timing chart when vertical transfer clock pulse is overlapping.

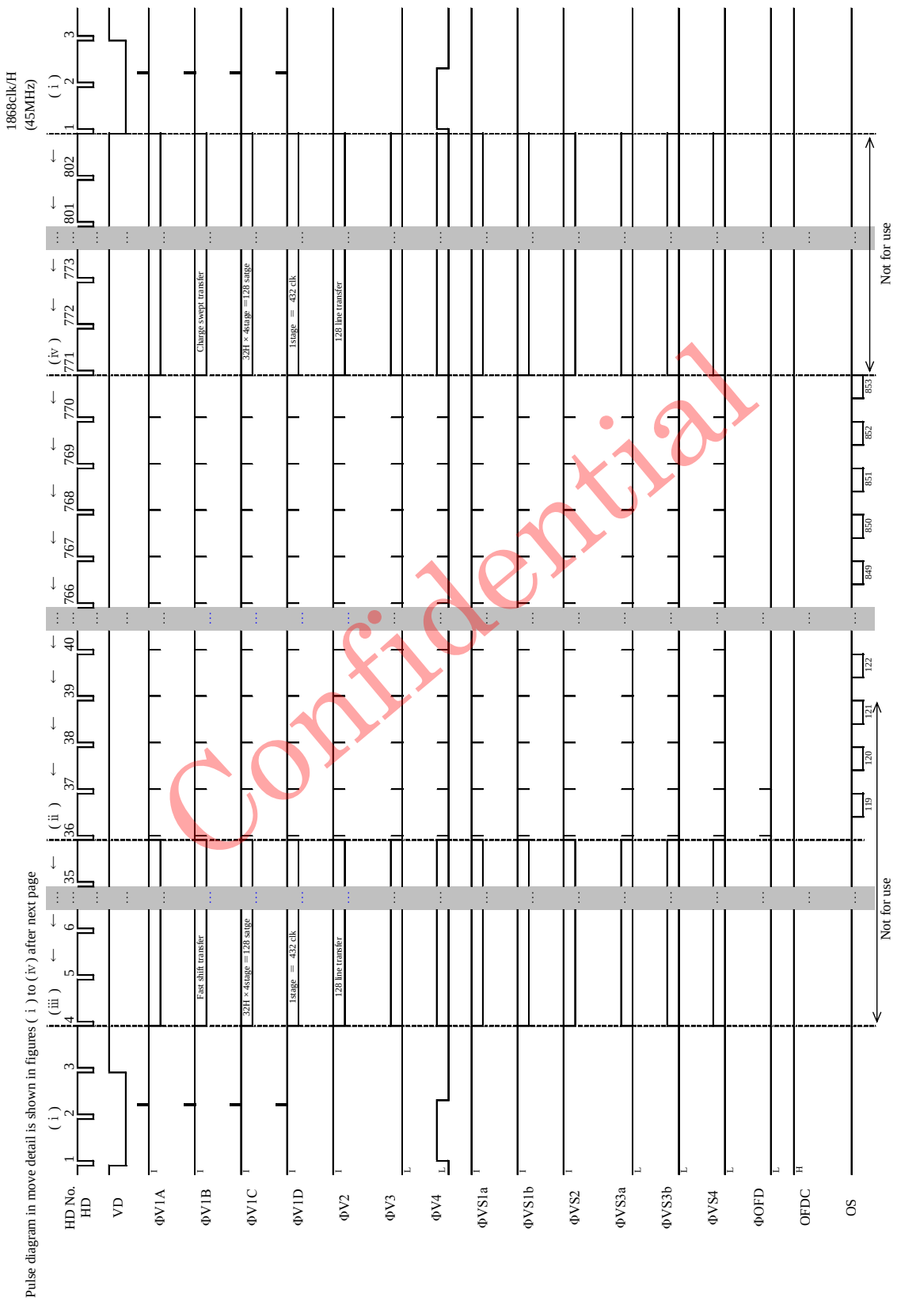
Horizontal transfer timing【 4-pixels addition(VGA), 60 frames/s 】(ii)



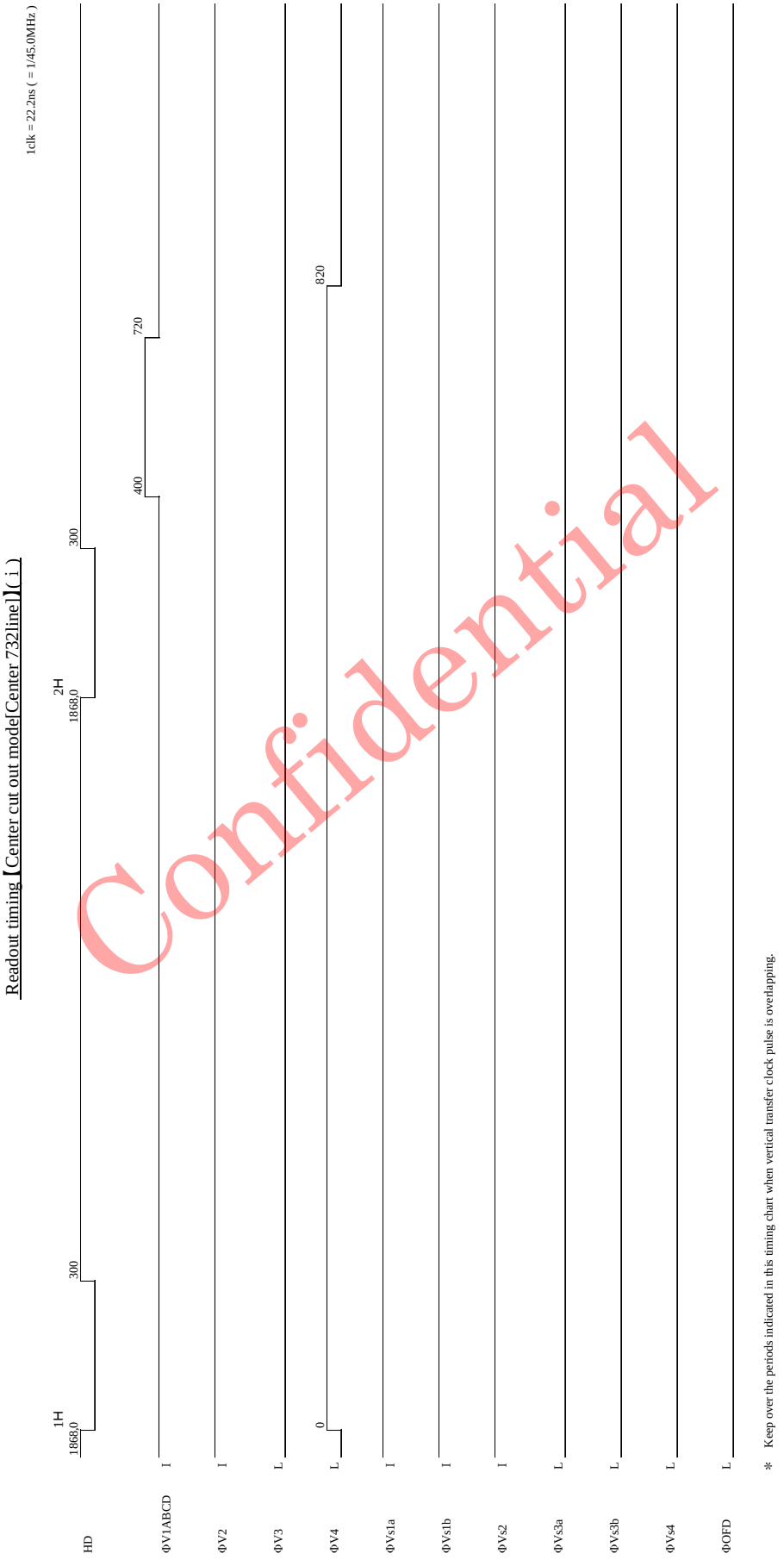
* Keep over the periods indicated in this timing chart when vertical transfer clock pulse is overlapping.

Vertical transfer timing【Center cut out mode[Center 732line]】

Pulse diagram in move detail is shown in figures (i) to (iv) after next page

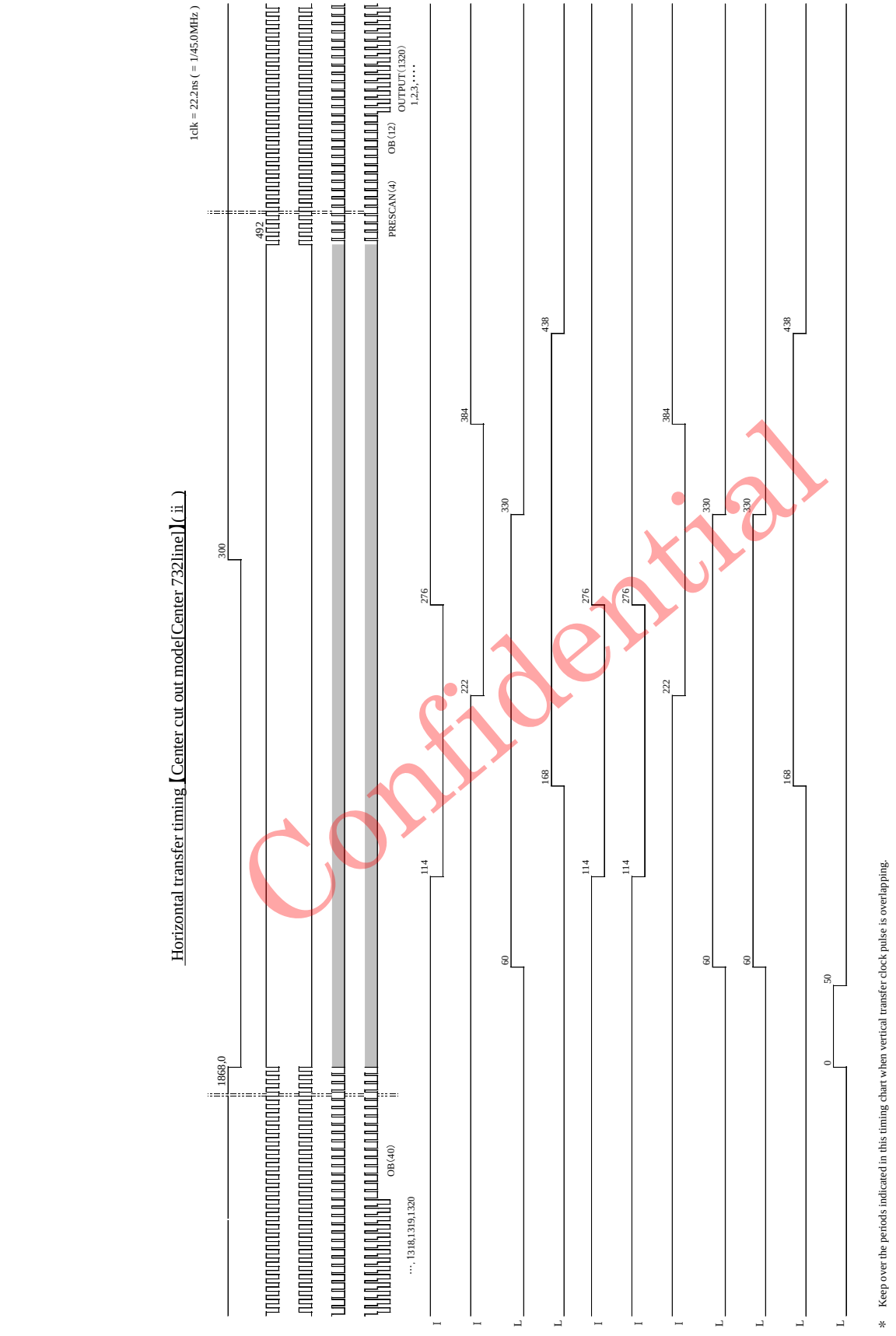


Readout timing【Center cut out mode(Center 732line)】(i)



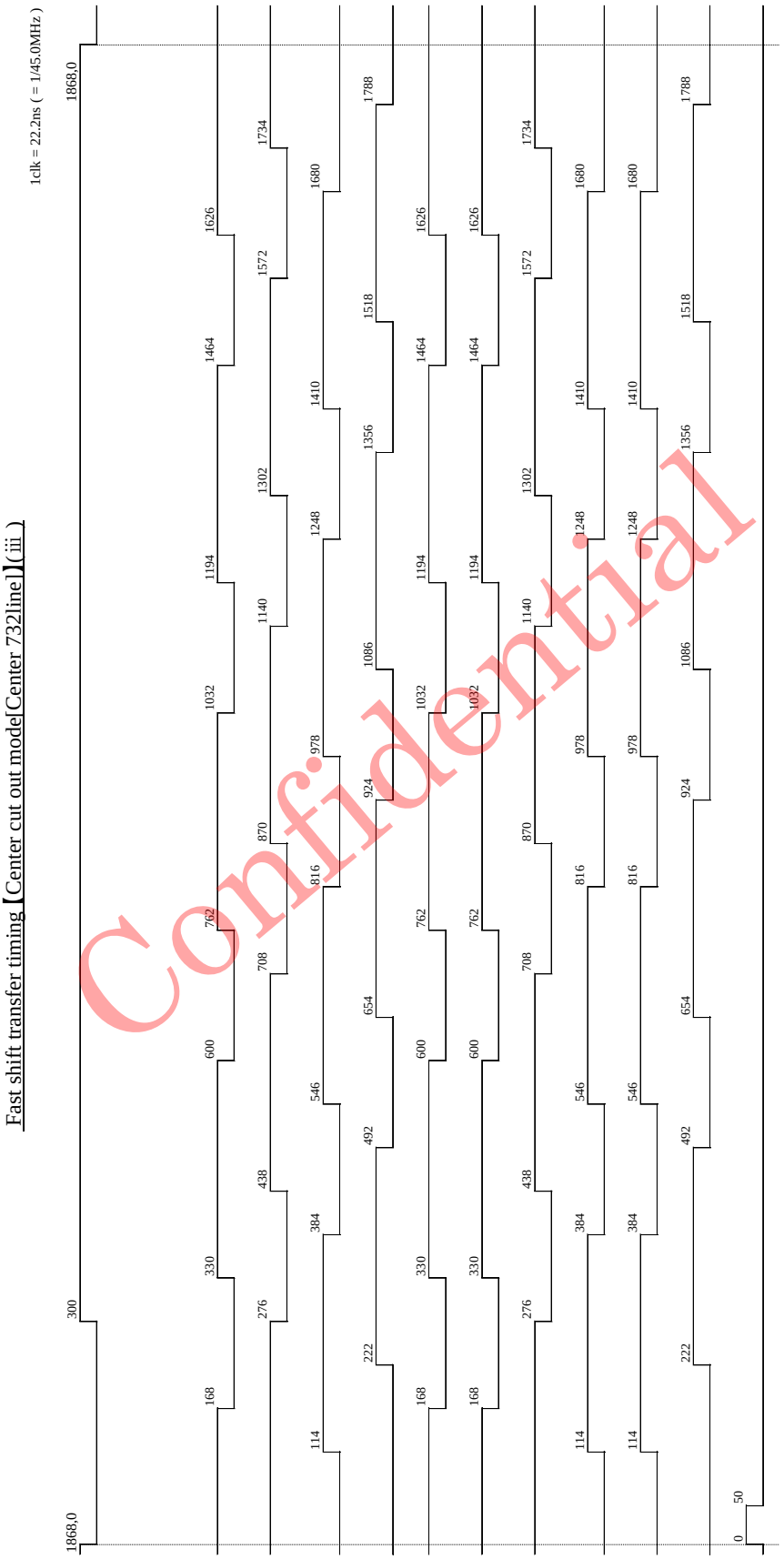
* Keep over the periods indicated in this timing chart when vertical transfer clock pulse is overlapping.

Horizontal transfer timing【Center cut out mode[Center 732line]】(ii)

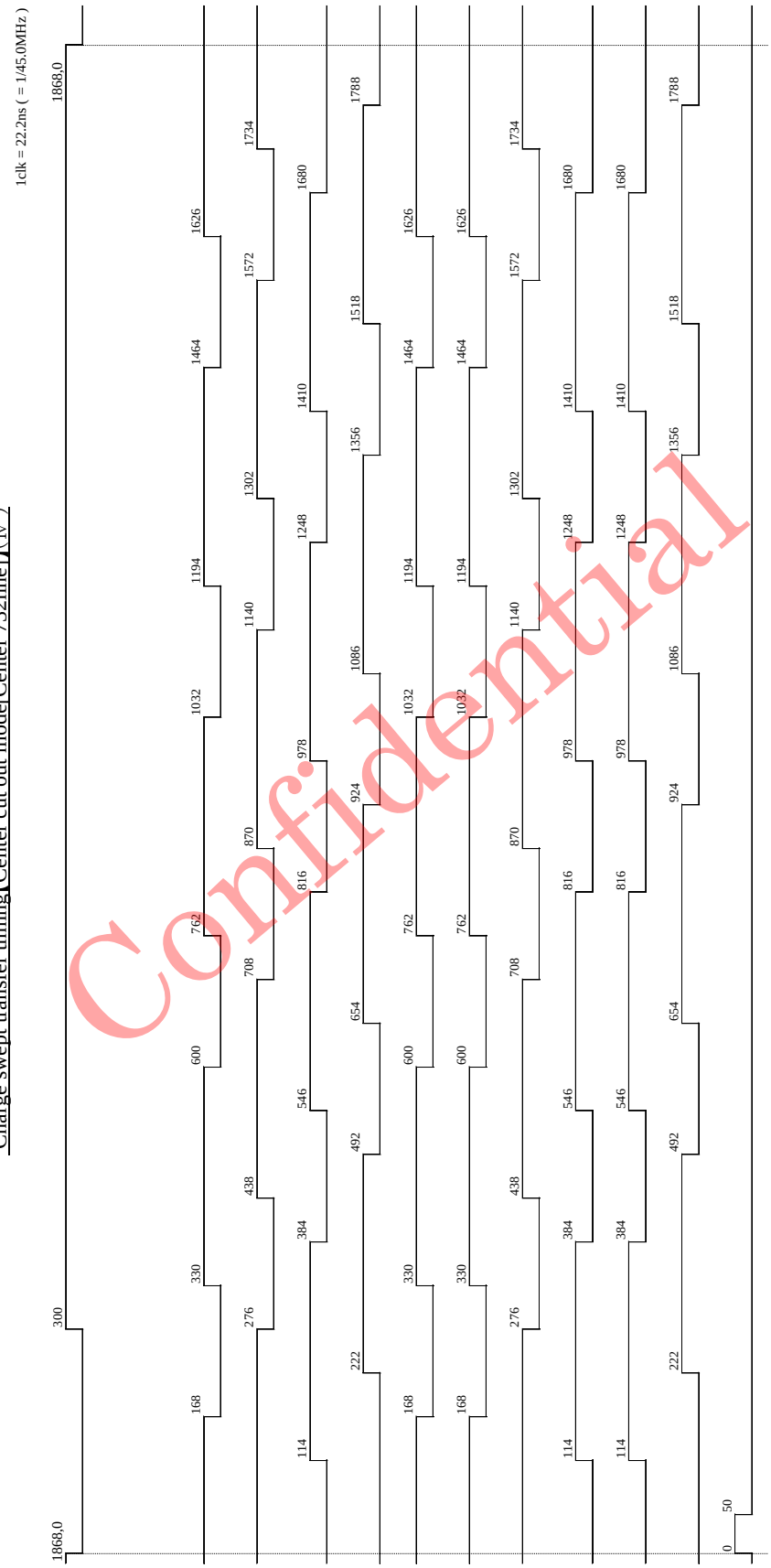


* Keep over the periods indicated in this timing chart when vertical transfer clock pulse is overlapping.

Fast shift transfer timing【Center cut out mode[Center 732line]】(iii)



* Keep over the periods indicated in this timing chart when vertical transfer clock pulse is overlapping.

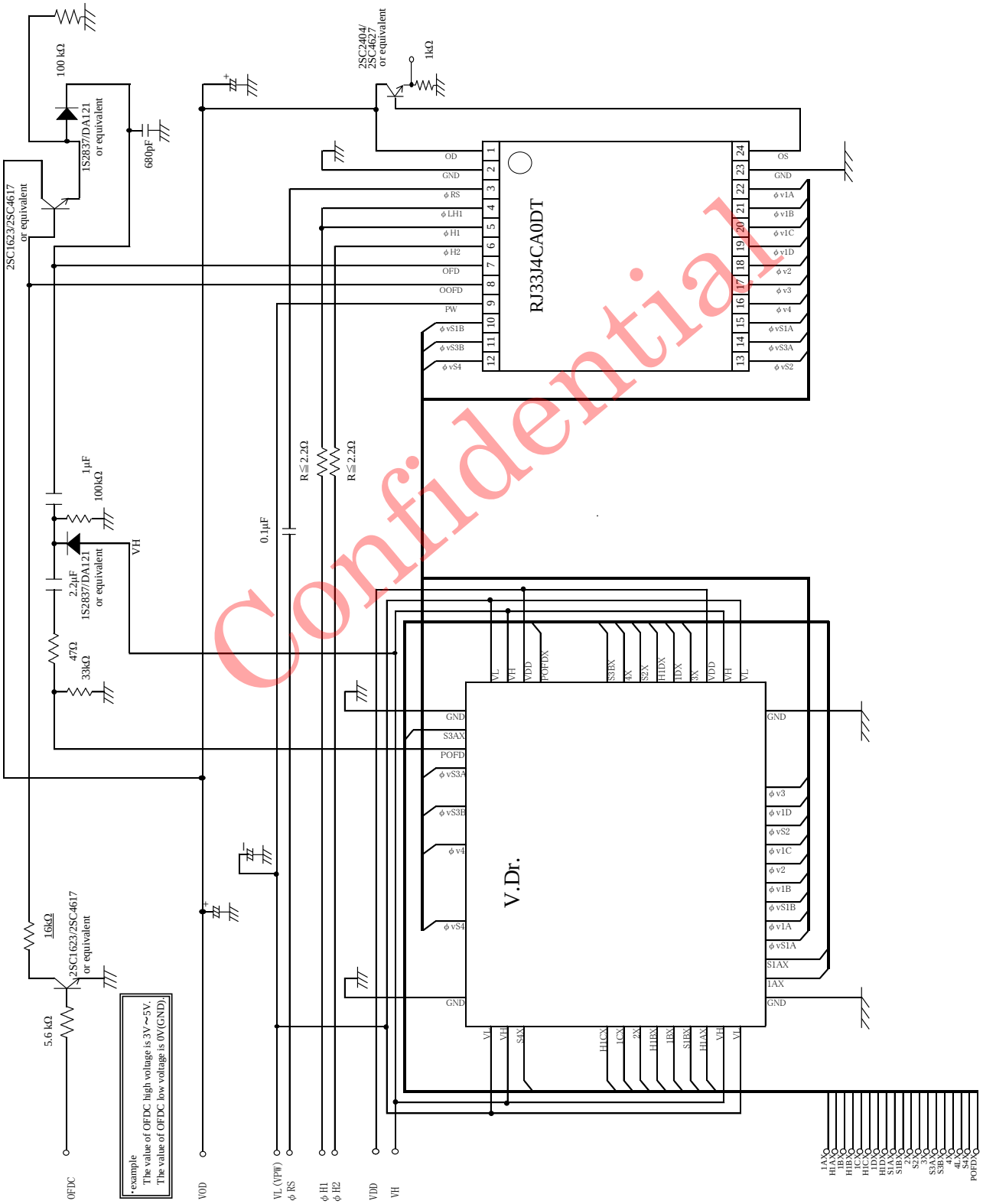


* Keep over the periods indicated in this timing chart when vertical transfer clock pulse is overlapping.

8 EXAMPLE OF STANDARD OPERATING CIRCUIT

・EXAMPLE OF OPERATING CIRCUIT-1

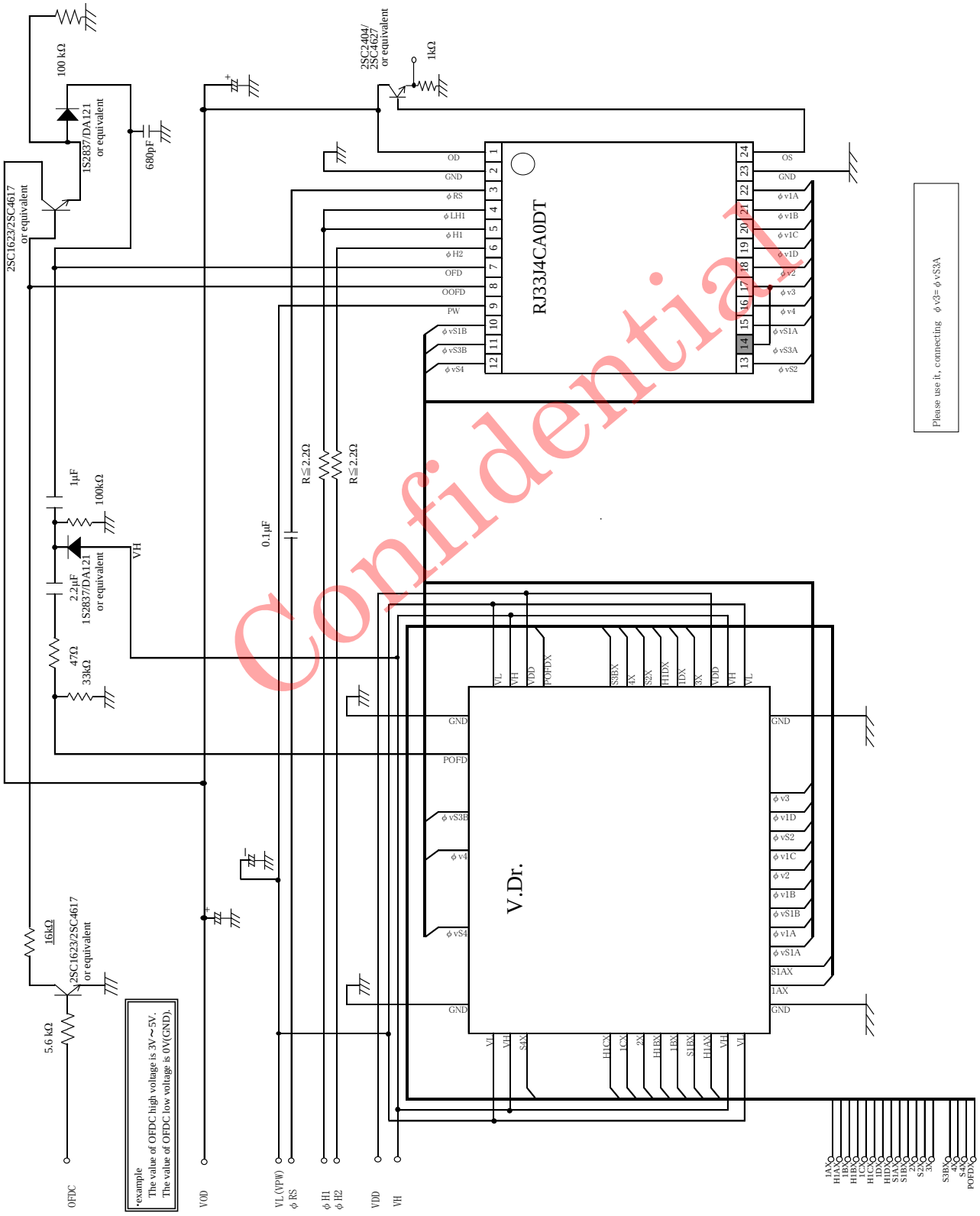
（For standard operatinng.）



・EXAMPLE OF OPERATING CIRCUIT-2

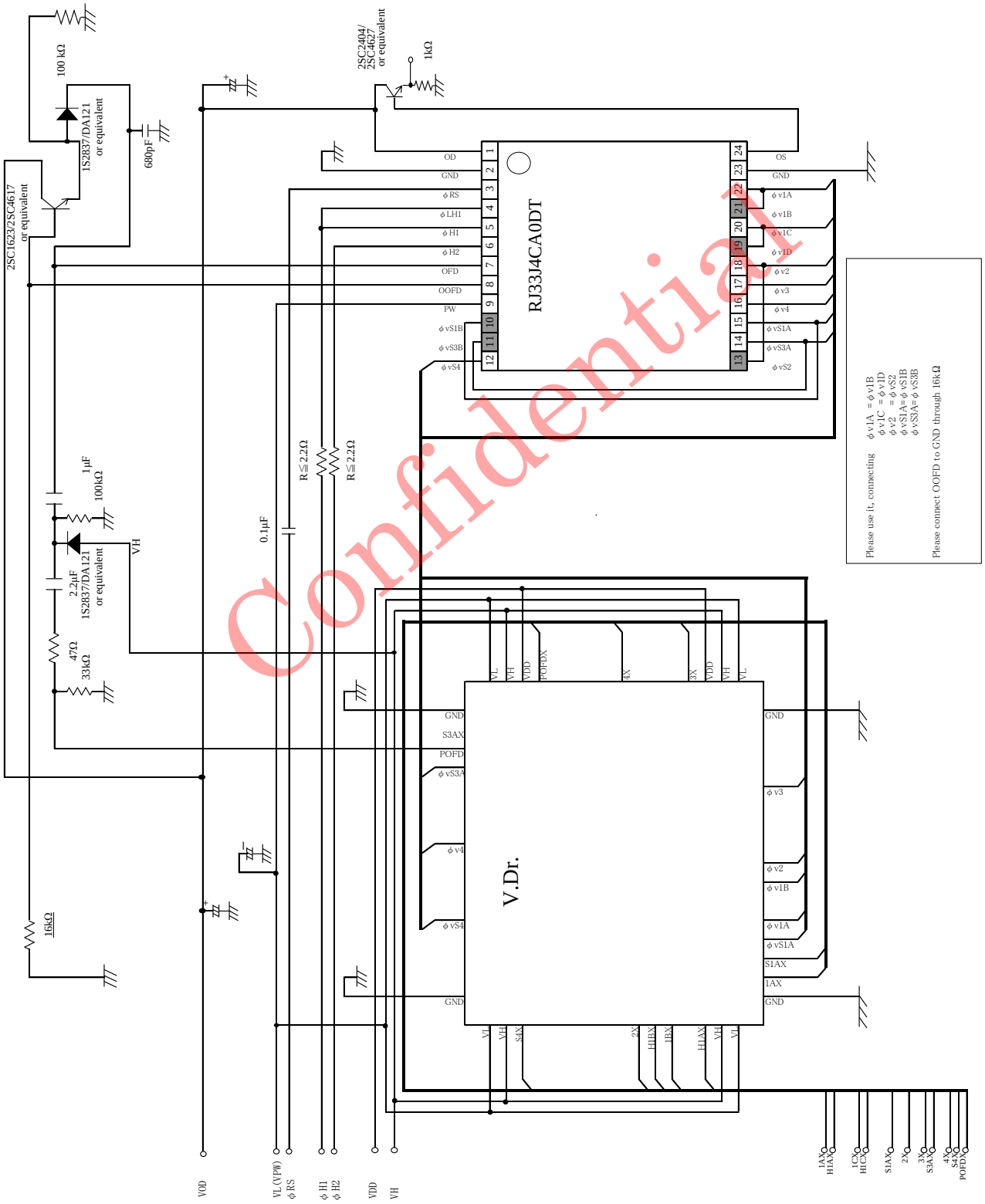
（When the number of φV terminals is 12, please connect in this example of a circuit.-2）

[Please use it, connecting φv3=φvS3A]



・EXAMPLE OF OPERATING CIRCUIT-3

（When the number of φV terminals is 8, please connect in this example of a circuit.-3
However, 4-pixels addition[VGA]60 frames/s -mode cannot be used in the example of the circuit-3.）
[Please use it, connecting φv1A = φv1B、 φv1C = φv1D、 φv2 = φvS2、 φvS1A= φvS1B、 φvS3A= φvS3B]



9 SPECIFICATION FOR BLEMISH（1/30 s frame accumulation）

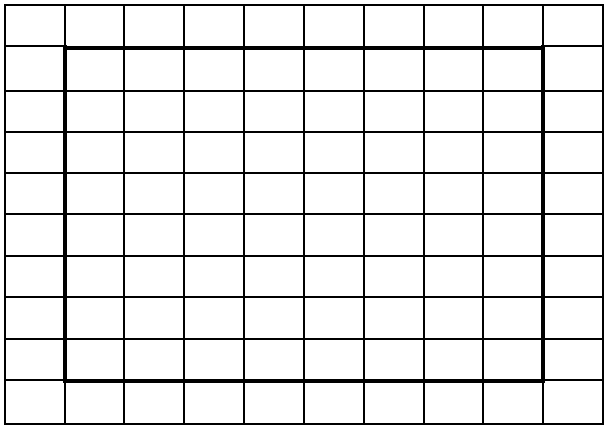
1） Definition of blemish

	Level of blemish (mV)	Permitted number of blemish	Comment
White blemish (Exposed)	100≦ B	0	・See fig.9-1(a), fig.9-2. ・Vout ＝ Vstd
	B ＜100	no count	
Black blemish (Exposed)	120≦ B	0	
	55≦ B ＜120	10	
	40≦ B ＜ 55	10	
	B ＜ 40	no count	
White blemish (Non-Exposed)	100＜ B	0	・See fig.9-1(b), fig.9-2 ・N≦40 ・M＋N≦200
	20＜ B ≦100	N	
	2.5＜ B ≦ 20	M	
	B ≦2.5	no count	
White blemish (Shutter mode)	5.0≦ B	0	・See fig.9-1(a), fig.9-2. ・Vout ＝ Vstd/10 ・The electronic shutter speed is set at 1/10000 s
	B ＜5.0	no count	
Black blemish (Shutter mode)	5.0≦ B	0	
	B ＜5.0	no count	

《note》 ・ B : Blemish level defined in fig. 9-1.
・ Vout : Average output voltage
・ Vstd : 150 mV (The average output voltage). The standard output voltage defined in the specification of the characteristics.

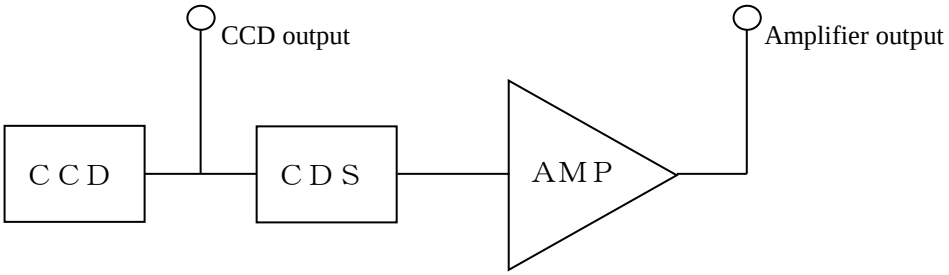
＊Total number of white blemish (non-exposed:20＜ B ≦100) and black blemish (exposed: 55≦ B ＜120)are less than 2 in arbitrary 8×8 pixels areas.

ex. The defects are less than 2 in the subsequent area surrounded by bold lines.



【MEASURING CONDITION】

・Ｔａ ： 60℃
・Measuring block diagram



The output voltage is measured at the CCD output.
The gain of the amplifier is adjusted to the unity between the CCD output and the amplifier output.

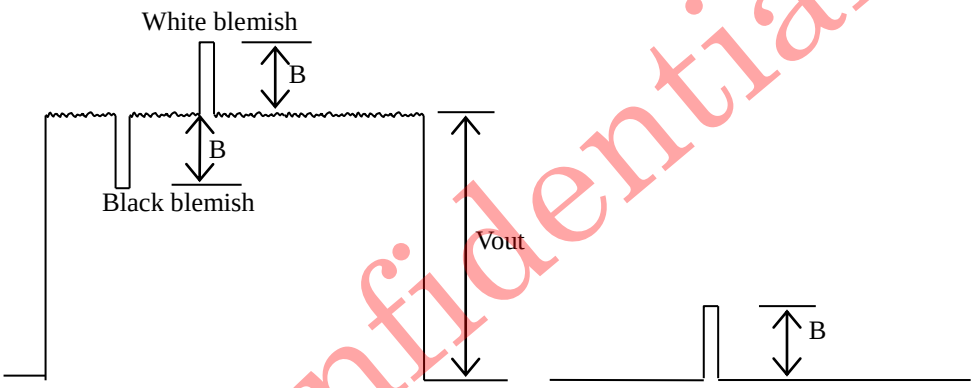


fig. 9-1 Definition of blemish level

(The wave form is the luminance signal measured at the Amplifier output)

【MEASURING AREA】

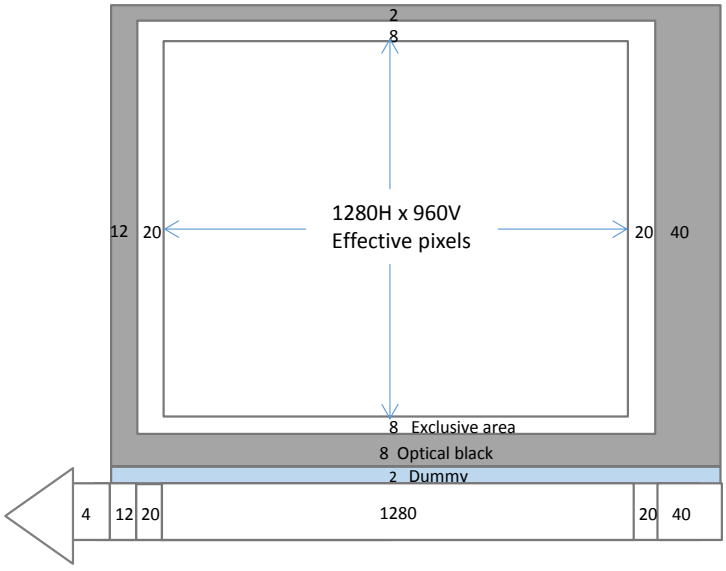


fig. 9-2 Definition of the measuring area

10 PRECAUTIONS

10.1 Package Breakage

In order to prevent the package from being broken, observe the following instructions:

1) The CCD is a precise optical component and the package material is plastic.
Therefore,
- Take care not to drop the device when mounting, handling, or transporting.
- Avoid giving a shock to the package. Especially when leads are fixed to the socket or the circuit board, small shock could break the package more easily than when the package isn't fixed.

2) When mounting the package on the housing, be sure that the package is not bent.
- If a bent package is forced into place between a hard plate or the like, the package may be broken.

3) If any damage or breakage occurs on the surface of the glass cap, its characteristics could deteriorate.
Therefore,
- Do not hit the glass cap.
- Do not give a shock large enough to cause distortion.
- Do not scrub or scratch the glass surface.
- Even a soft cloth or applicator, if dry, could cause flaws to scratch the glass.

10.2 Electrostatic Damage

As compared with general MOS-LSI, CCD has lower ESD.
Therefore, take the following antistatic measures when handling the CCD:

1) Always discharge static electricity by grounding the human body and the instrument to be used.
To ground the human body, provide resistance of about 1 MΩ between the human body and the ground to be on the safe side.
2) When directly handling the device with the fingers, hold the part without leads and do not touch any lead.
3) To avoid generating static electricity,
a. do not scrub the glass surface with cloth or plastic
b. do not attach any tape or labels
c. do not clean the glass surface with dust-cleaning tape
4) When storing or transporting the device, put it in a container of conductive material.

10.3 Dust and Contamination

Dust or contamination on the glass surface could deteriorate the output characteristics or cause a scar.
In order to minimize dust or contamination on the glass surface, take the following precautions：

1） Handle the CCD in a clean environment such as a cleaned booth.（The cleanliness level should be, if possible, class 1,000 at least.）

2） Do not touch the glass surface with the fingers. If dust or contamination gets on the glass surface, the following cleaning method is recommended：

・Dust from static electricity should be blown off with an ionized air blower.
For anti-electrostatic measures, however, ground all the leads on the device before blowing off the dust.

・The contamination on the glass surface should be wiped off with a clean applicator soaked in Isopropyl alcohol. Wipe slowly and gently in one direction only.

－ Frequently replace the applicator and do not use the same applicator to clean more than one device.

※ Note：n most cases, dust and contamination are unavoidable, even before the device is first used. It is, therefore, recommend that the above procedures should be taken to wipe out dust and contamination before using the device.

10.4 Other

1） Soldering should be manually performed within 5 seconds at 350℃ maximum at the tip of soldering iron.

2） Avoid using or storing the CCD at high temperature or high humidity as it is a precise optical component. Do not give a mechanical shock to the CCD.

3） CCD has the possibility that white blemish, which originates in the structure of CCD with the passage of time by an external factor such as the radiations, could be generated.
Please use white blemish compensation circuit for white blemish generated afterward.

11 PACKAGE OUTLINE AND PACKING SPECIFICATION

11 1. Package Outline Specification

Refer to attached drawing.

(The seal resin stick out from the package shall be passed. And, the seal resins are two kinds of colors, while and transparency.)

11 2. Markings

Marking contents

(1). Product name : RJ33J4CA0DT

(2). Company name : SHARP

(3). Country of origin : JAPAN

(4). Date code : YY WW X XX

- XX: Denotes the production ref. code.(2 figures)
- X: Denotes the production day of the week.

1	2	3	4	5	6	7
SUN.	MON.	TUE.	WED.	THU.	FRI.	SAT.

- WW: Denotes the production week. (01,02,03,…,52,53)
- YY: Denotes the production year. (Lower two digits of the year.)

Positions of markings are shown in the package outline drawing.
But, markings shown in that drawing are not provided any measurements of their characters and their positions.

11 3. Packing Specification

3-1. Packing materials

Material Name	Material Spec.	Purpose
Cover Tape	Plastic film(1device/tape)	Glass lid covering
Device case	Cardboard(540devices/case)	Device tray fixing
Device tray	Conductive plastic (90devices/tray)	Device packing(6trays/case)
Cover tray	Conductive plastic(1tray/case)	Device packing
PP band	Polypropylene	Device tray fixing
Buffer	Cardboard(2sheets/case)	Shock absorber of device tray
Plastic film bag	Plastic film	Device tray fixing
Tape	Paper	Sealing plastic film bag and device case
Label	Paper	Indicates part number, quantity and date of manufacture

3-2. External appearance of packing

Refer to attached drawing

11 4. Precaution

1). Before unpacking, confirm the imports of the chapter "Handling Precaution" in this device specification.

2). Unpacking should be done on the stand treated with anti-ESD. At that time, the same anti-ESD treatment should be done to operator's body, too.

11 5. Chemical substance information in the product

Product Information Notification based on Chinese law, Management Methods for Controlling Pollution by Electronic Information Products.

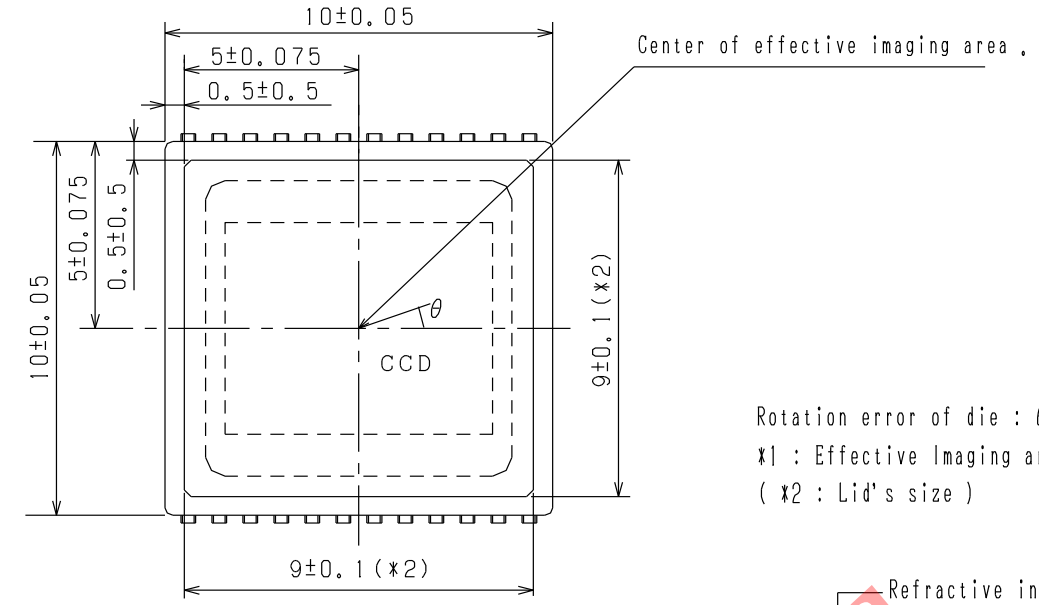
Names and Contents of the Hazardous Substances.

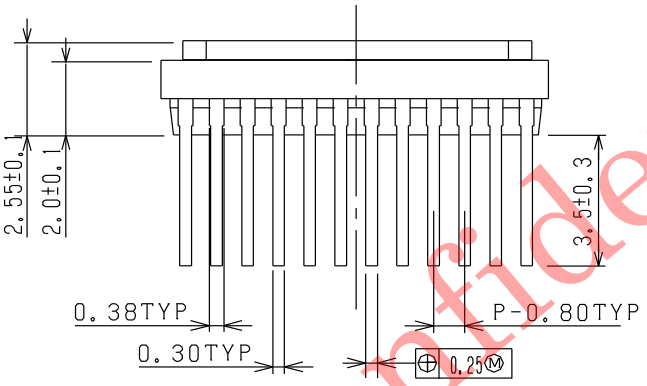
Hazardous Substances					
Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
○	○	○	○	○	○

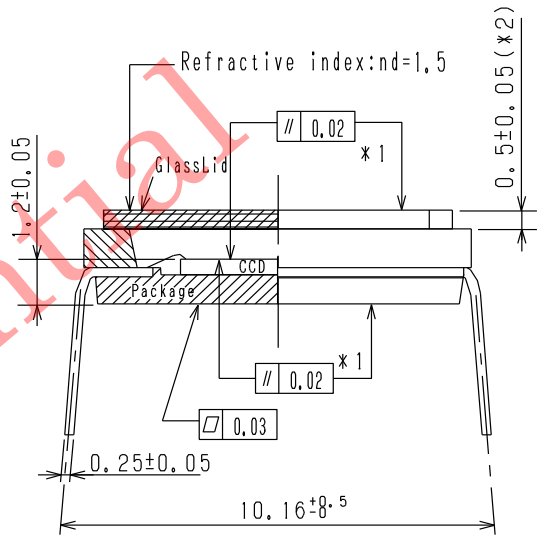
This table is prepared in accordance with the provisions of SJ/T 11364.

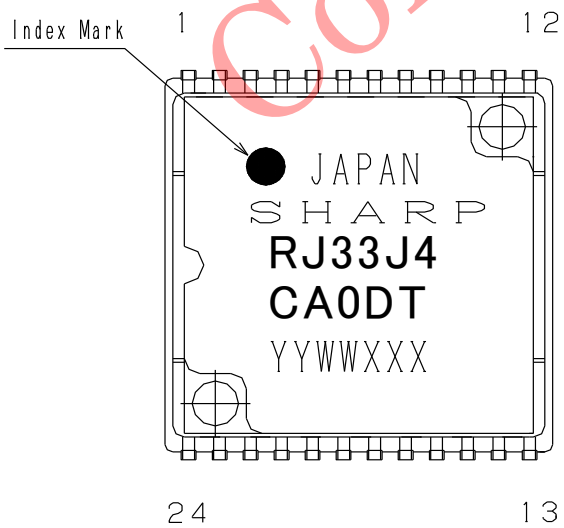
○ : Indicates that said hazardous substance contained in all of the homogeneous materials for this part is below the limit requirement of GB/T 26572.

× : Indicates that said hazardous substance contained in at least one of the homogeneous materials used for this part is above the limit requirement of GB/T 26572.



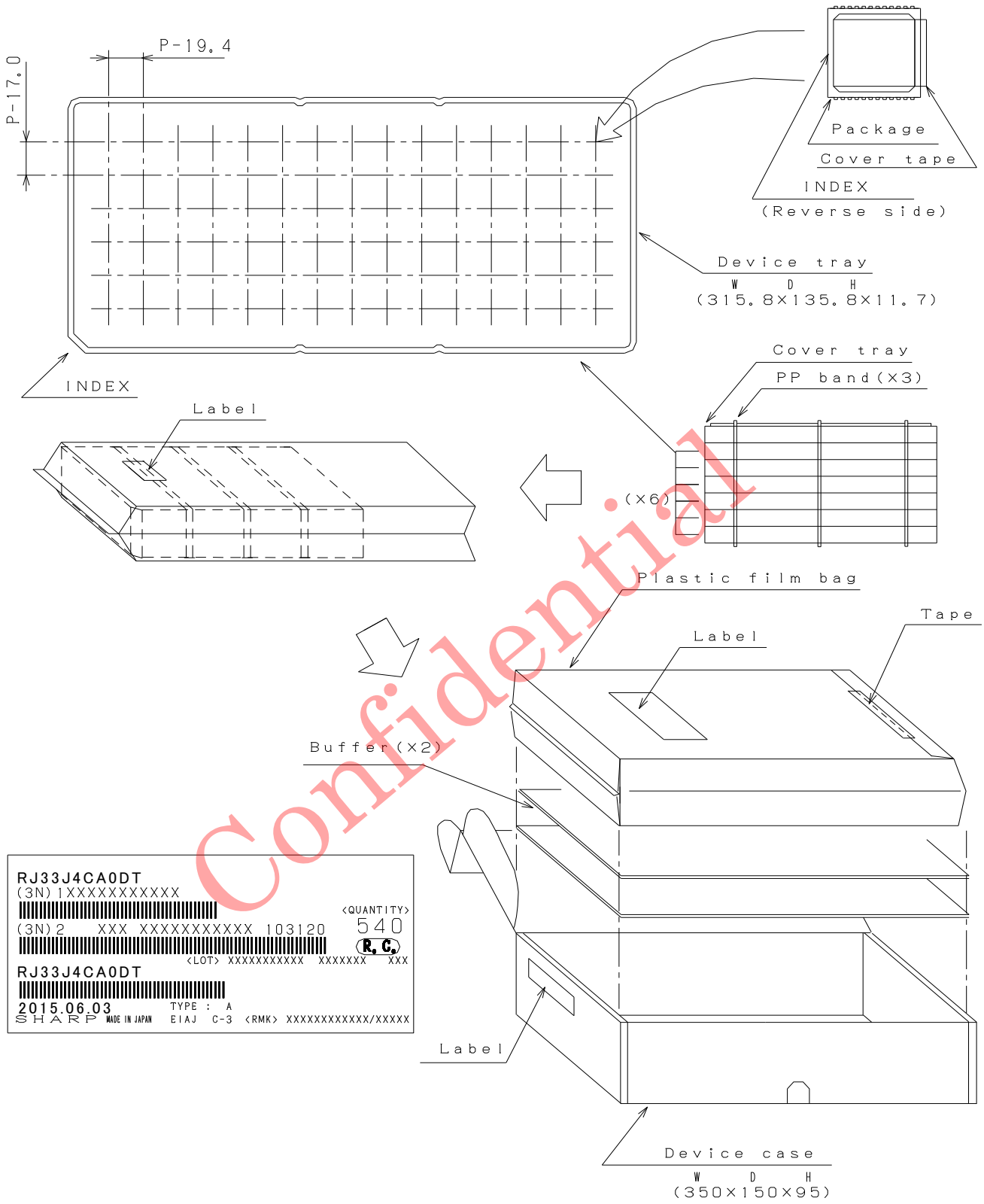






(UNIT:mm)

材質MATERIAL	仕上 FINISH	名 称 NAME	WDIP24-P-400 Package Outline Specification
		コード CODE	
Assembly Process Production Engineering Dept. I			
ELECTRONIC COMPONENTS AND DEVICES GROUP		図 番 DRAWING No.	GDP024A-17E2A
SHARP CORPORATION			



(UNIT:mm)

材質 MATERIAL	仕上 FINISH	名称 NAME	External Appearance of Packing
		コード CODE	
Assembly Process Production Engineering Dept. I			
ELECTRONIC COMPONENTS AND DEVICES GROUP		図番 DRAWING No.	KSEC-540T4-9
SHARP CORPORATION			