SHARP

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To : _____

PRELIMINARY

SPECIFICATIONS

Product Type 1/1.8-type Progressive Scan Color CCD Area Sensor with 2106k Pixels

Model No R J 3 1 N 3 A D 0 D T

※ This specifications contains 42 pages including the cover and appendix.
If you have any objections, please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

DATE : _____

BY : _____

PRESENTED

BY : J. Nakai

J.NAKAI
Dept. General Manager

SHARP CORPORATION
SENSING DEVICE UNIT DEV. DEPT. II
Jun 3 2013
MAIL DATE
ELECTRONIC COMPONENTS AND DEVICES DIVISION

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Sensing Device Unit
Electronic Components And Devices Division
SHARP CORPORATION

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Office electronics
- Instrumentation and measuring equipment
- Machine tools
- Audiovisual equipment
- Home appliance
- Communication equipment other than for trunk lines

(3) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.
- Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
- Mainframe computers
- Traffic control systems
- Gas leak detectors and automatic cutoff devices
- Rescue and security equipment
- Other safety devices and safety equipment, etc

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- Aerospace equipment
- Communications equipment for trunk lines
- Control equipment for the nuclear power industry
- Medical equipment related to life support, etc.

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○ Please direct all queries and regarding the products covered herein to a sales representative of the company.

CONTENTS

RJ31N3AD0DT

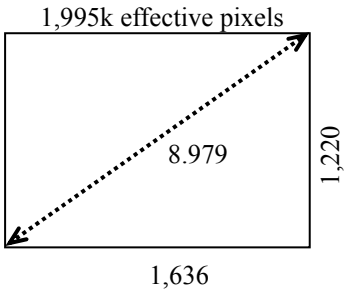
1/1.8-type Progressive Scan Color CCD Area Sensor with 2132k Pixels

1 DESCRIPTION

The RJ31N3AD0ET is a 1/1.8-type solid-state image sensor that consists of PN photo-diodes and CCDs（charge-coupled devices）. With approximately 2,132,000 pixels, the sensor provides a high resolution stable color image.

1 . 1 Features

1）Optical size : 8.979 mm（Aspect ratio 4：3）
2）Progressive scan format
3）Square pixel
4）Number of total pixels : Horizontal 1708× vertical 1248
Number of image pixels : Horizontal 1644 × vertical 1236
Number of effective pixels : Horizontal 1636 × vertical 1220
Pixel pitch : Horizontal 4.4 μ m × vertical 4.4 μ m
Number of optical black pixels : Horizontal；32 front and 32 rear
: Vertical ；10front and 2 rear
Number of dummy bits : Horizontal；8 front and 8 rear , Vertical；1 front
5）R, G and B primary color mosaic filters
6）Supports monitoring mode
7）Built-in overflow drain voltage output circuit, and reset gate voltage circuit
8）Variable electronic shutter
9）Low fixed pattern noise and lag
10）No burn-in and no image distortion
11）Blooming suppression structure
12）Built-in output amplifier
13）N-type silicon substrate, N-MOS process,
Not designed or rated as radiation hardened
14）Global shutter



1 . 2 Applications

1）Electronic still cameras, video capturing devices for PCs, etc
2）Pattern recognition

iSHCCD™ in iSHartina™

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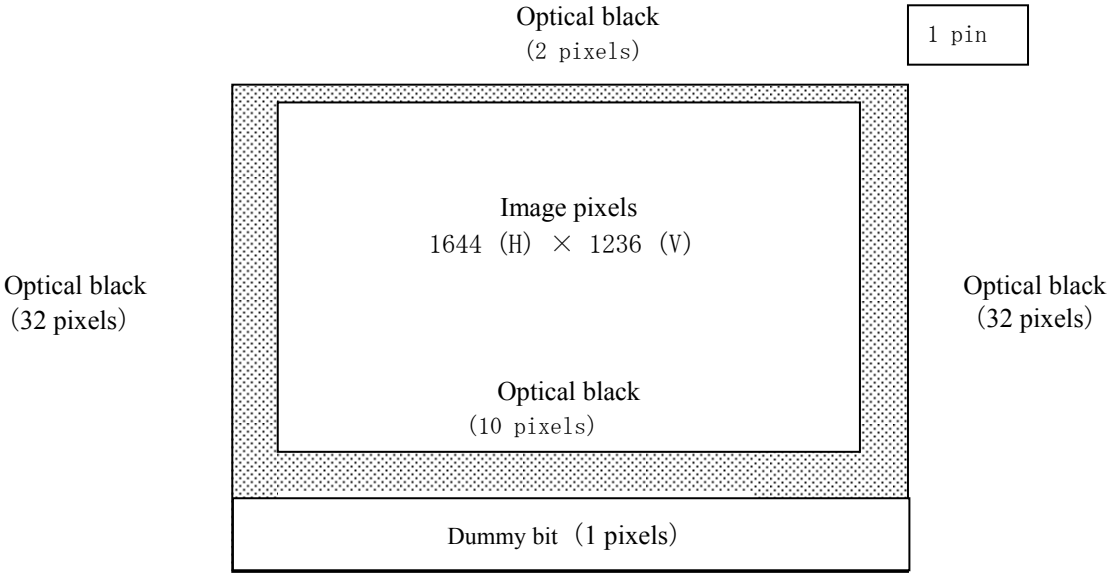
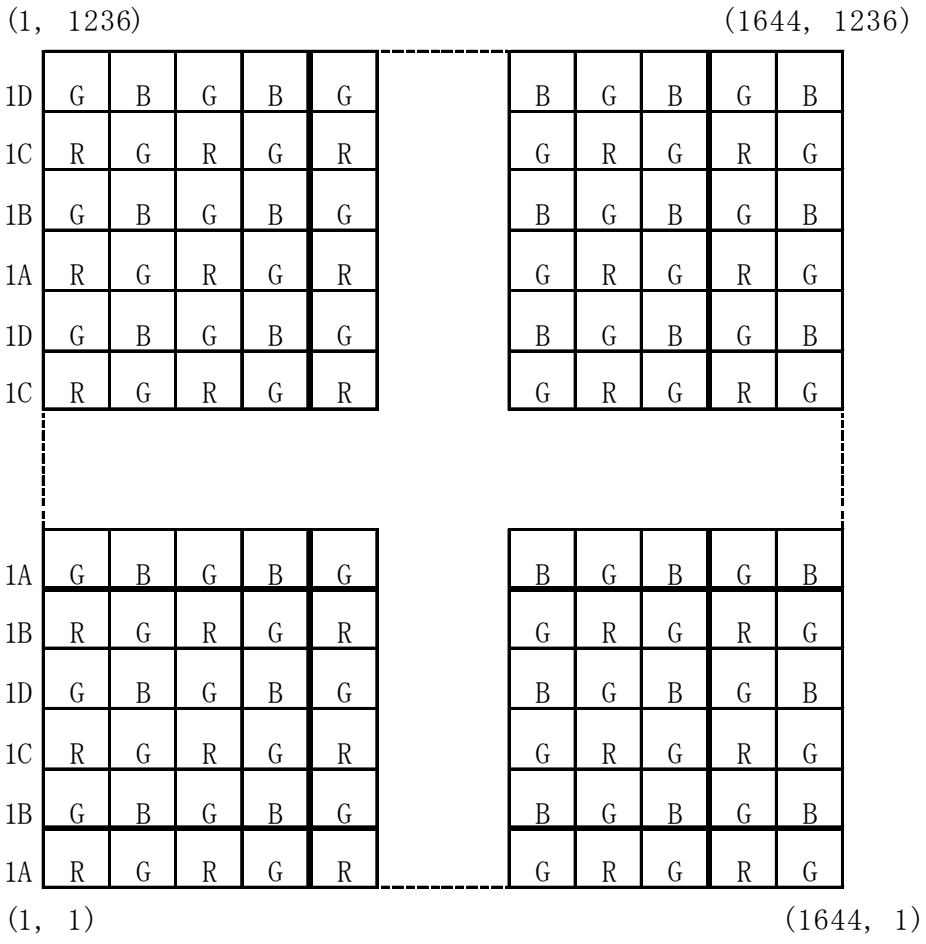
The "iSHCCD" is a CCD image sensor that introduced high-sensitivity and high-efficiency technologies developed by Sharp.
The "iSHartina" series is a key device group of Sharp which realizes a next-generation sensing world.

The circuit diagram and others included in this specifications are intended for use to explain typical application examples. Therefore, we take no responsibility for any problem as may occur due to the use of the included circuit and for any problem with industrial proprietary rights or other rights.

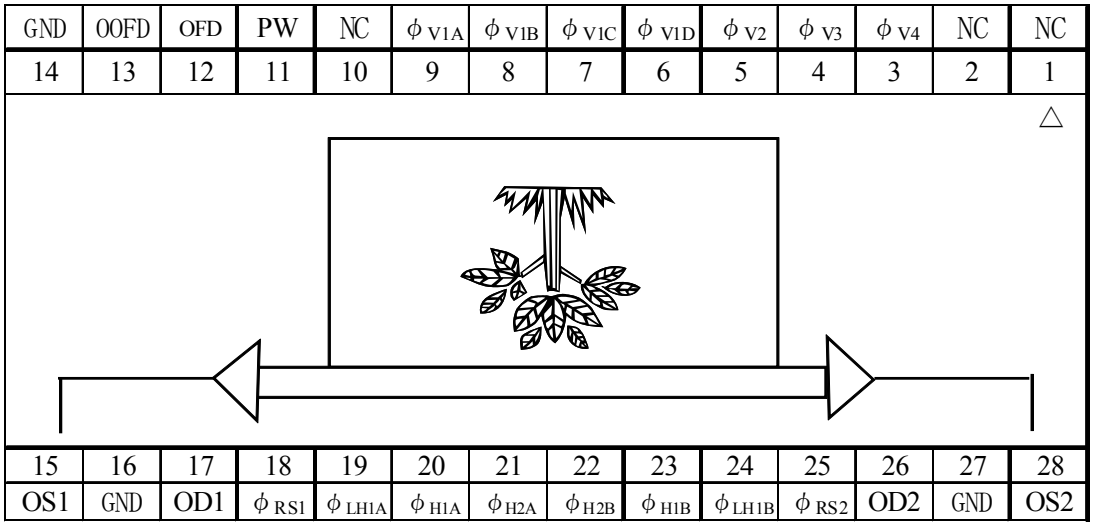
2 ARRANGEMENT OF PIXELS AND COLOR FILTERS



Pin arrangement of the vertical readout clock



3 PIN CONFIGURATION (TOP VIEW)



Symbol	Pin name
OD1,OD2	Output transistor drain
OS1,OS2	Output signals
ϕ_{RS1}, ϕ_{RS2}	Reset transistor clock
ϕ_{V1A}, ϕ_{V1B}, ϕ_{V1C}, ϕ_{V1D}, ϕ_{V2}, ϕ_{V3}, ϕ_{V4},	Vertical shift register clock
ϕ_{LH1A}, ϕ_{LH1B}, ϕ_{H1A}, ϕ_{H2A}, ϕ_{H1B}, ϕ_{H2B}	Horizontal shift resister clock
OFD	Overflow drain
OOFD	Output overflow drain
PW	P_well
GND	Ground

4 ABSOLUTE MAXIMUM RATINGS

(T_A=25℃)

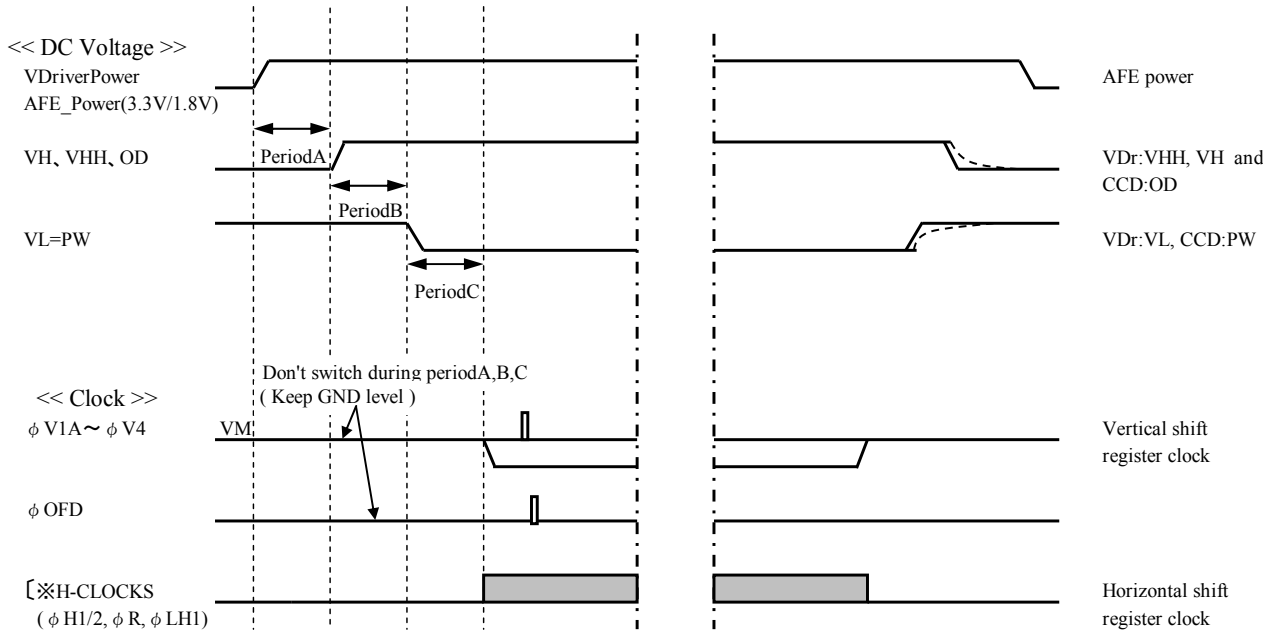
Parameter	Symbol	Ratings	Unit
Output transistor drain voltage	V_{OD}	0 to +15.4	V
Overflow drain voltage	V_{OFD}	Internal output (Note 1)	
Reset gate clock voltage	$V_{\phi RS}$	Internal output (Note 2)	
Vertical shift register clock voltage	$V_{\phi V}$	V_{PW} to +15.4	V
Horizontal shift register clock voltage	$V_{\phi H}$	-0.3 to +5.1	V
Voltage difference between P_well and vertical clock	V_{PW}-$V_{\phi V}$	-23.8 to +0	V
Voltage difference between vertical clocks	$V_{\phi V}$-$V_{\phi V}$	0 to +9.9 (Note 3)	V
Storage temperature	T_{STG}	-40 to +80	℃
Ambient operating temperature	T_{OPR}	-20 to +70	℃

(Note 1) Do not connect to DC voltage directly. When OFD is connected to GND, connect V_{OD} to GND. Overflow drain clock is applied below 22.5 Vp-p.

(Note 2) Do not connect to DC voltage directly. When ϕ_{RS} is connected to GND, connect V_{OD} to GND. Reset gate clock is applied below 5.1 Vp-p.

(Note 3) When clock width is below 10 μs, and clock duty factor is below 0.1 %, voltage difference between adjoining vertical clocks are guaranteed up to 15.4 V.
Do not change all ϕ_V during 0.5 μs before rising edge of $V_{\phi VH}$ pulse and after falling edge of $V_{\phi VH}$ pulse.
Do not change directly into $V_{\phi VL} \rightarrow V_{\phi VH}$ or $V_{\phi VH} \rightarrow V_{\phi VL}$.

4.1 CCD, VDr Power sequence



○Power ON sequence

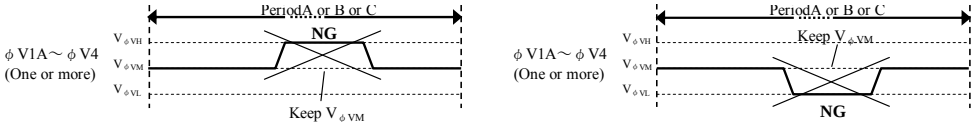
Turn on power in order of VDD→VH(=VHH=OD)→VL(=PW) and after that apply the clocks.
All φV pin of CCD should be VM[Intermediate(0V)]level during period A ,B,C.
φOFD pin of CCD should be Low level during period A ,B,C.
Period A : Turn on VH with the condition that all φV pulse is VM[Intermediate(0V)]level.
Period B : Turn on VL(=PW) after VH(=VHH=OD) voltage reach to higher than 90% of its typical voltage.
Period C : Start φV clocks after VL(=PW) voltage reach to lower than 90% of its typical voltage.

○Power OFF sequence

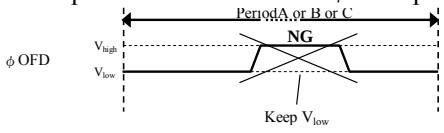
Turn off power in reverse order of Power ON. At Power OFF sequence, it is not problem any power reach to 0V earlier (caused by difference of time constant of decoupling capacitor).
But in case of turn on again, turn on should be done in order shown above after all voltage of power reach less than 10% of its typical value.
(AFE power < AFE power *0.1 & VH < VH*0.1 & VL > VL*0.1)

○Restriction matter of φV and φOFD switching

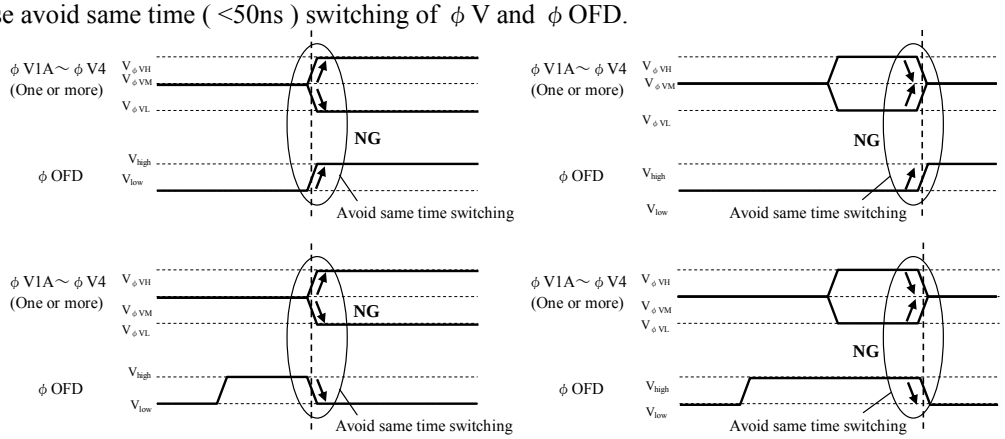
1) Please turn on power in condition that all φV pulse is VM[Intermediate(0V)]level.



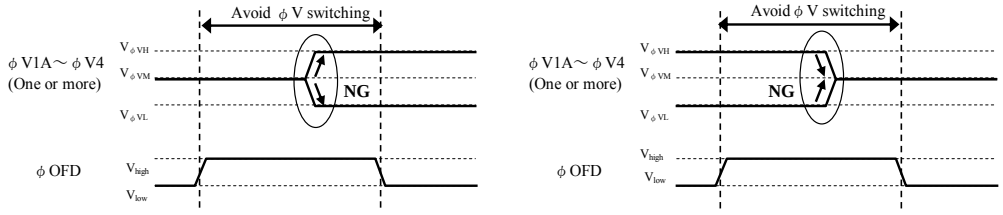
2) Please turn on power in condition that φOFD pulse is Low level.



3) Please avoid same time (<50ns) switching of ϕ V and ϕ OFD.

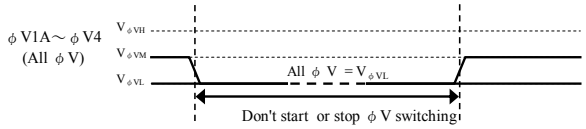


4)Please avoid switching of ϕ V during period that ϕ OFD is High.

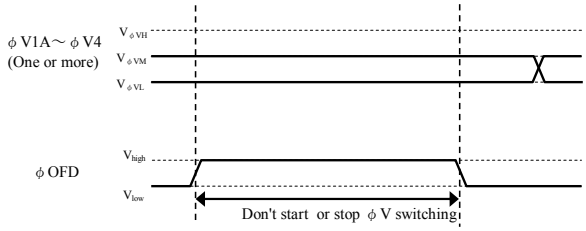


5) Start or stop ΦV switching at the arbitrary point on timing chart of CCD spec. except following period.
ϕ V clock should not start or stop at,

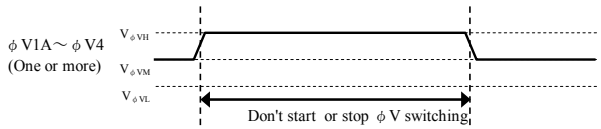
5-1)Exposure period of long time exposure (all ϕ V =L)



5-2)During period that ϕ OFD=High.

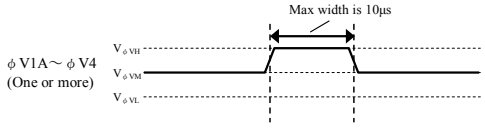


5-3)During period that ϕ V=High.

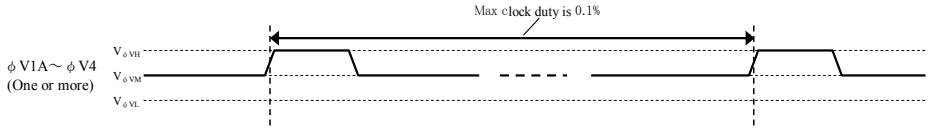


6) Only in case of clock width is below 10µs and clock duty factor is below 0.1%, voltage difference between adjoining vertical clocks are guaranteed up to 15.4V.
Only if all the following conditions are satisfied, VH pulse is allowed.

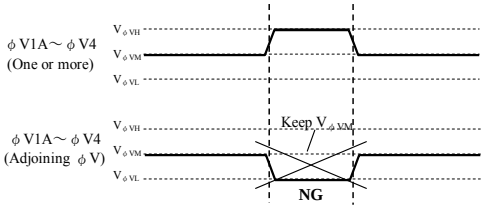
6-1) Width is 10µs or less.



6-2) Clock duty factor is 0.1% or less.

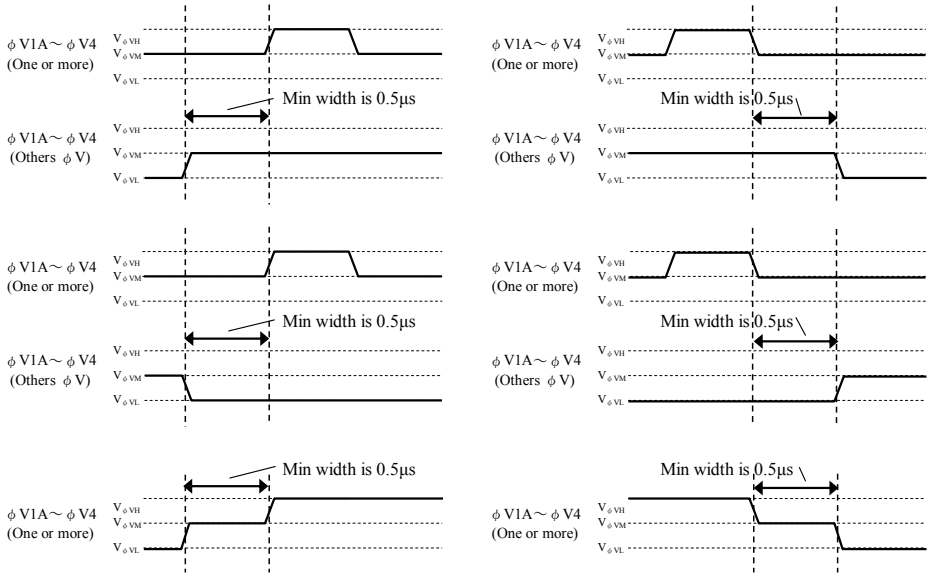


6-3) Ajoining gate level is 0V.

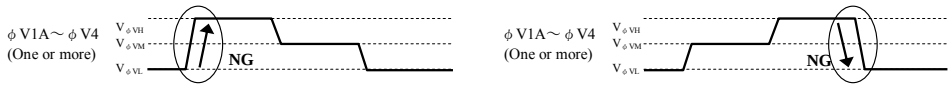


Adjoining vertical clock gate: See Table.1

7) Don't change all φV during 0.5µs before rising edge of VφVH pulse and after falling edge of VφVH pulse.



8) Don't change φV directly into VφVL→VφVH or VφVH → VφVL.



9) Please change mode follow timing chart in CCD spec.

* This sequence explanation specify at Sharp CCD pin. Please check with AFE vender about sequence of AFE.

		Adjoining pin						
		V1A	V1B	V1C	V1D	V2	V3	V4
ΦVpin	V1A					○		○
	V1B					○		○
	V1C					○		○
	V1D					○		○
	V2	○	○	○	○		○	
	V3					○		○
	V4	○	○	○	○		○	

Table.1 Information for adjoining Vertical clock gate pin (ΦVpin)

5 RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min.	Typ.	Max.	Unit
Ambient operating temperature		T_{OPR}		25.0		℃
Output transistor drain voltage		V_{OD1},V_{OD2},	13.1	13.5	13.9	V
Overflow drain clock	p-p level（Note 1）	$V_{\phi OFD}$	19.3	20.0	20.7	V
Ground		GND		0.0		V
P_well voltage	（Note 2）	V_{PW}	-6.8		$V_{\phi VL}$	V
Vertical shift register Clockaoji	LOW level	$V_{\phi V1AL}$, $V_{\phi V1BL}$, $V_{\phi V1CL}$, $V_{\phi V1DL}$, $V_{\phi V2L}$, $V_{\phi V3L}$, $V_{\phi V4L}$,	-6.8	-6.5	-6.2	V
	INTERMEDIATE level	$V_{\phi V1AI}$, $V_{\phi V1BI}$, $V_{\phi V1CI}$, $V_{\phi V1DI}$, $V_{\phi V2I}$, $V_{\phi V3I}$, $V_{\phi V4I}$,		0.0		V
	HIGH level	$V_{\phi V1AH}$, $V_{\phi V1BH}$, $V_{\phi V1CH}$, $V_{\phi V1DH}$	13.1	13.5	13.9	V
Horizontal shift register clock	LOW level	$V_{\phi LH1LA}$, $V_{\phi LH1LB}$, $V_{\phi H1AL}$,$V_{\phi H2AL}$, $V_{\phi H1BL}$,$V_{\phi H2BL}$	-0.05	0.0	0.05	V
	HIGH level	$V_{\phi LH1HA}$, $V_{\phi LH1HB}$, $V_{\phi H1AH}$,$V_{\phi H2AH}$, $V_{\phi H1BH}$,$V_{\phi H2BH}$	3.15		3.6	V
Reset gate clock	p-p level（Note 1）	$V_{\phi RS1}$,$V_{\phi RS2}$	3.15		3.6	V
Vertical shift register clock frequency （Note 3）		$f_{\phi V1A}$,$f_{\phi V1B}$, $f_{\phi V1C}$,$f_{\phi V1D}$, $f_{\phi V2}$,$f_{\phi V3}$,,$f_{\phi V4}$		37.5		KHz
Horizontal shift register clock frequency		f_{LH1},f_{LH2}, f_{H1A},f_{H2A},f_{H1B},f_{H2B}		40.0		MHz
Reset gate clock frequency		$f_{\phi RS1}$,$f_{\phi RS2}$,		40.0		MHz

（Note 1） Use the circuit parameter indicated in “7 EXAMPLE OF STANDARD OPERATING CIRCUIT” (P.23), and do not connect to DC voltage directly.

（Note 2） V_{PW} is set below $V_{\phi VL}$ that is low level of vertical shift register clock, or is used with the same power supply that is connected to V_L of V driver IC.

（Note 3） At frame accumulation mode.

※ To apply power, first connect GND and then turn on V_{OD}. After turning on V_{OD}, turn on V_{PW} first and then turn on other powers and pulses.
Do not connect the device to or disconnect it from the plug socket while power is being applied.

6 CHARACTERISTICS（Drive method：1/30s frame accumulation）

T_A：+25℃, but +60℃ for parameter No.4 and No.5.
Operating conditions：the typical values specified in “5 RECOMMENDED OPERATING CONDITIONS”.
Color temperature of light source：3200K, IR cut-off filter（CM-500,1 mmt）is used.

No.	Parameter	Symbol	Note	Minimum	Typical	Maximum	Unit
1	Standard output voltage	V_O	1		150		mV
2	Photo response non-uniformity	PRNU	2			10	%
3	Saturation output voltage	V_{SAT}	3	TBD			mV
4	Dark output voltage	V_{DARK}	4		0.5	3.0	mV
5	Dark signal non-uniformity	DSNU	5		0.5	2.0	mV
6	Sensitivity（Green channel）	R（G）	6		1100		mV
7	Smear ratio	SMR	7		-120		dB
8	Image lag	AI	8			1.0	%
9	Blooming suppression ratio	ABL	9	1000			
10	Output transistor drain current	I_{OD}			6.0	9.0	mA

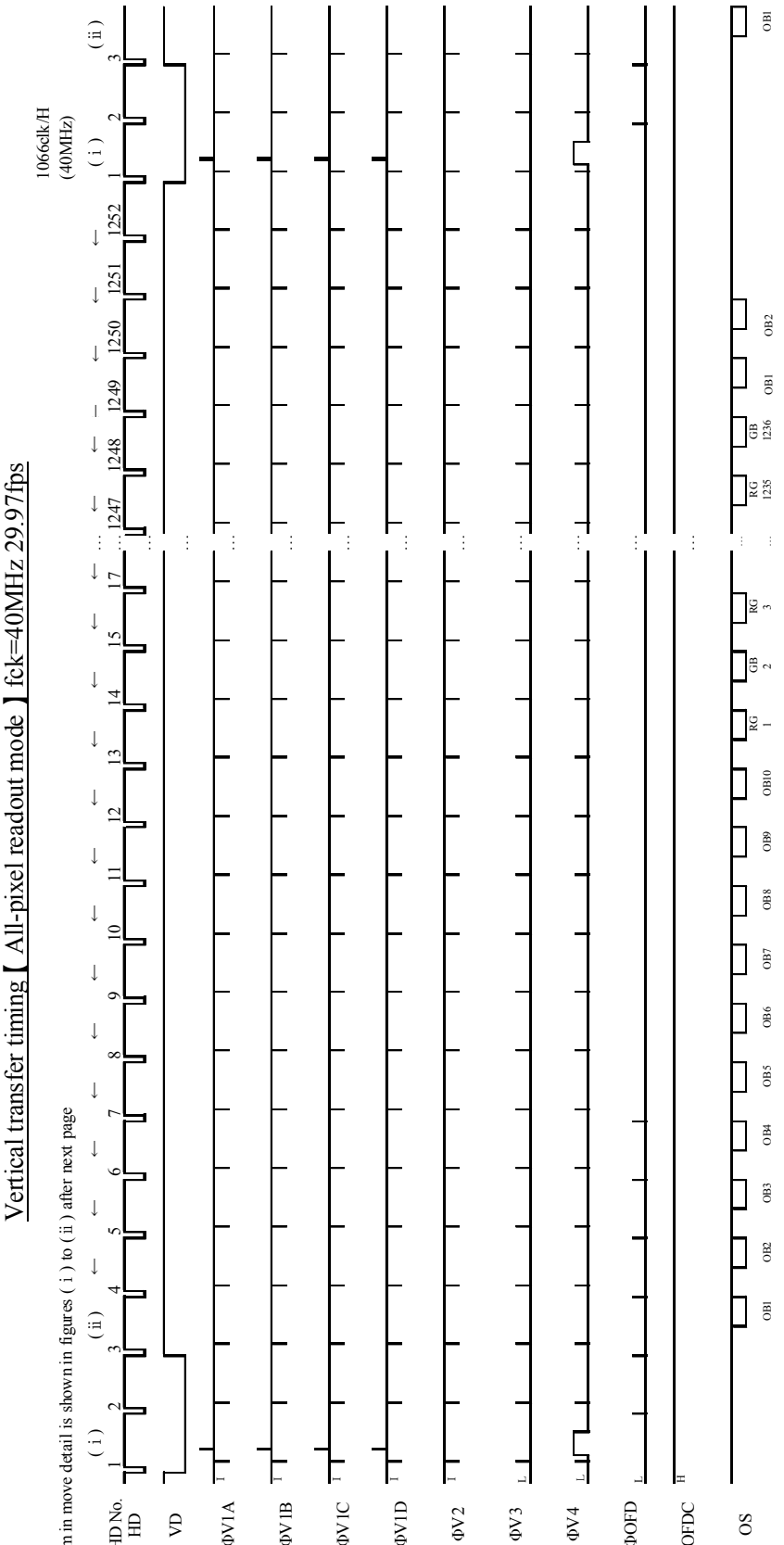
【 Notes 】

1 The average output voltage of G signal under the uniform illumination. The standard exposure conditions are defined as when V_O is 150 mV.
2 The image area is divided into 10 × 10 segments under the standard exposure conditions. Each segment’s voltage is the average output voltage of all pixels within the segment. PRNU is defined by （Vmax - Vmin） / V_O, where Vmax and Vmin are the maximum and minimum values of each segment’s voltage respectively.
3 The image area is divided into 10 × 10 segments. Each segment’s voltage is the average output voltages of all pixels within the segment. Vsat is the minimum segment’s voltage under 10 times exposure of the standard exposure conditions.
4 The average output voltage under non-exposure conditions.
5 The image area is divided into 10 × 10 segments under non-exposure conditions. DSNU is defined by（Vdmax – Vdmin）, where Vdmax and Vdmin are the maximum and minimum values of each segment’s voltage respectively.
6 The average output voltage of G signal when a 1000 lux light source with a 90 % reflector is imaged by a lens of F4, f50 mm.
7 The sensor is exposed only in the central area of V/10 square with a lens at F4, where V is the vertical image size. SMR is defined by the ratio of the output voltage detected during the vertical blanking period to the maximum output voltage in the V/10 square.
8 The sensor is exposed at the exposure level corresponding to the standard conditions. AI is defined by the ratio of the output voltage measured at the 1st field during the non-exposure period to the standard output voltage.
9 The sensor is exposed only in the central area of V/10 square, where V is the vertical image size. ABL is defined by the ratio of the exposure at the standard conditions to the exposure at a point where blooming is observed.

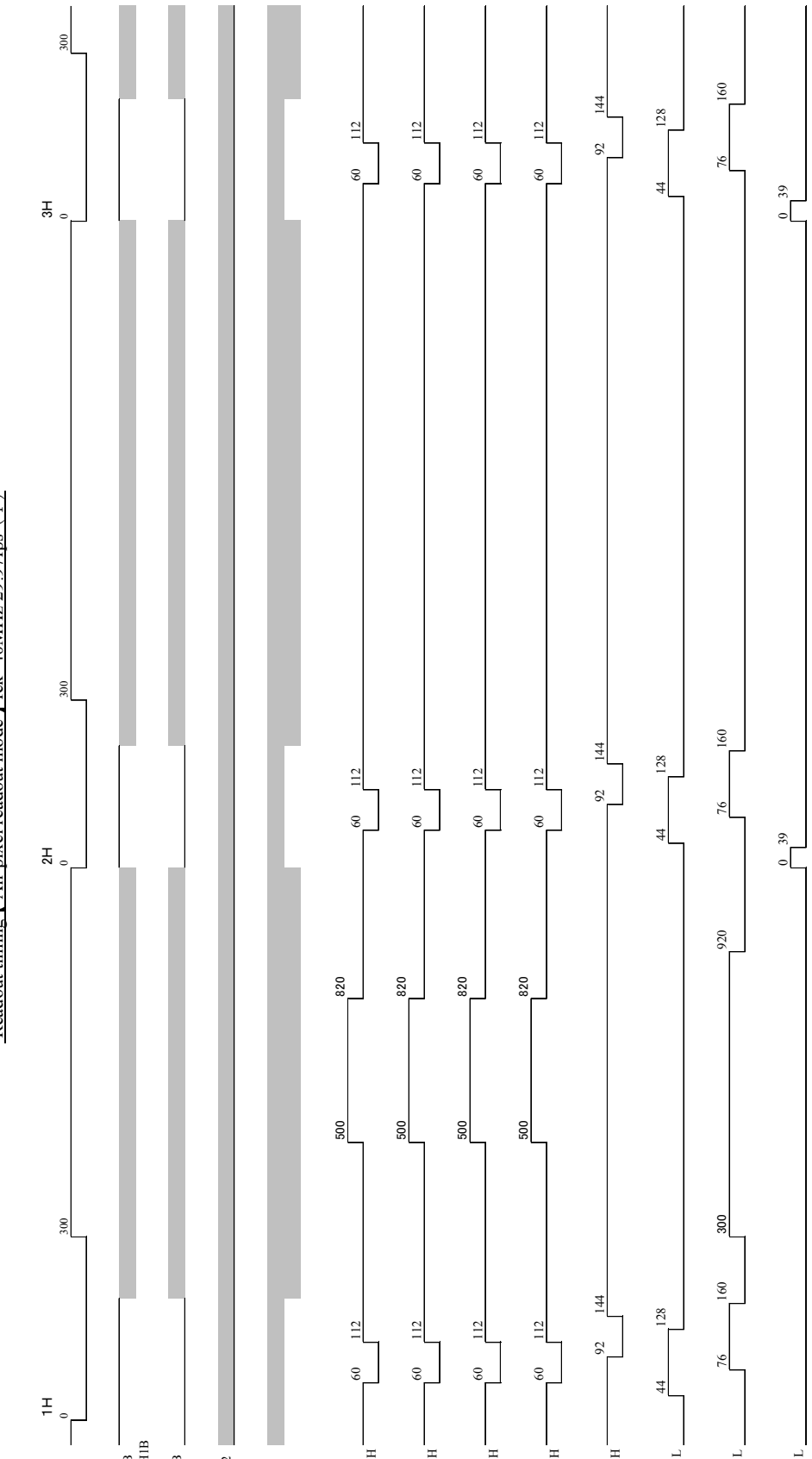
【 Comment 】

Within the recommended operating conditions of V_{OD}, V_{OFD} of the internal output satisfies with ABL and V_{SAT}.

7 DRIVE TIMING CHART

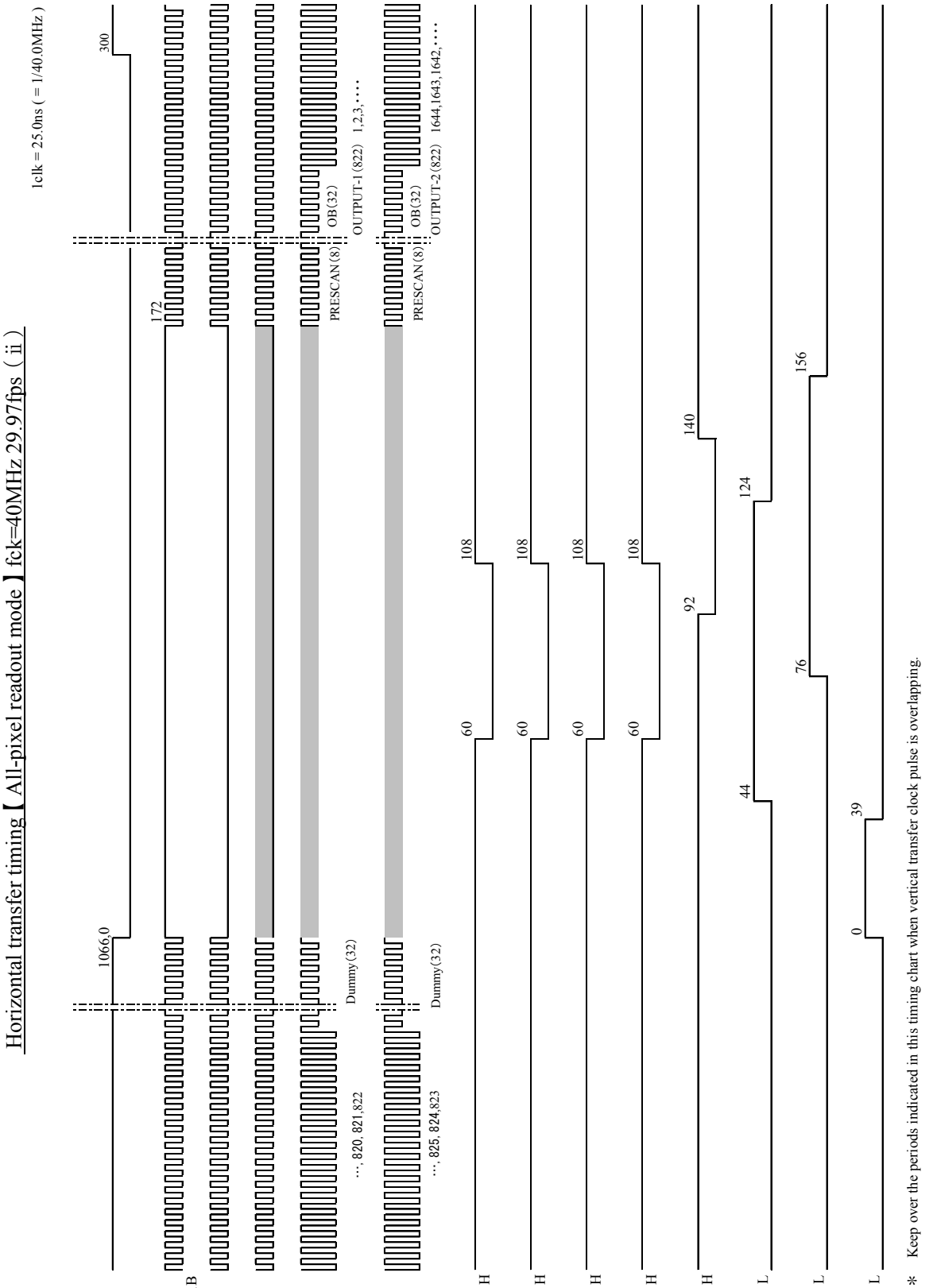


Readout timing【All-pixel readout mode】fck=40MHz 29.97fps（i）

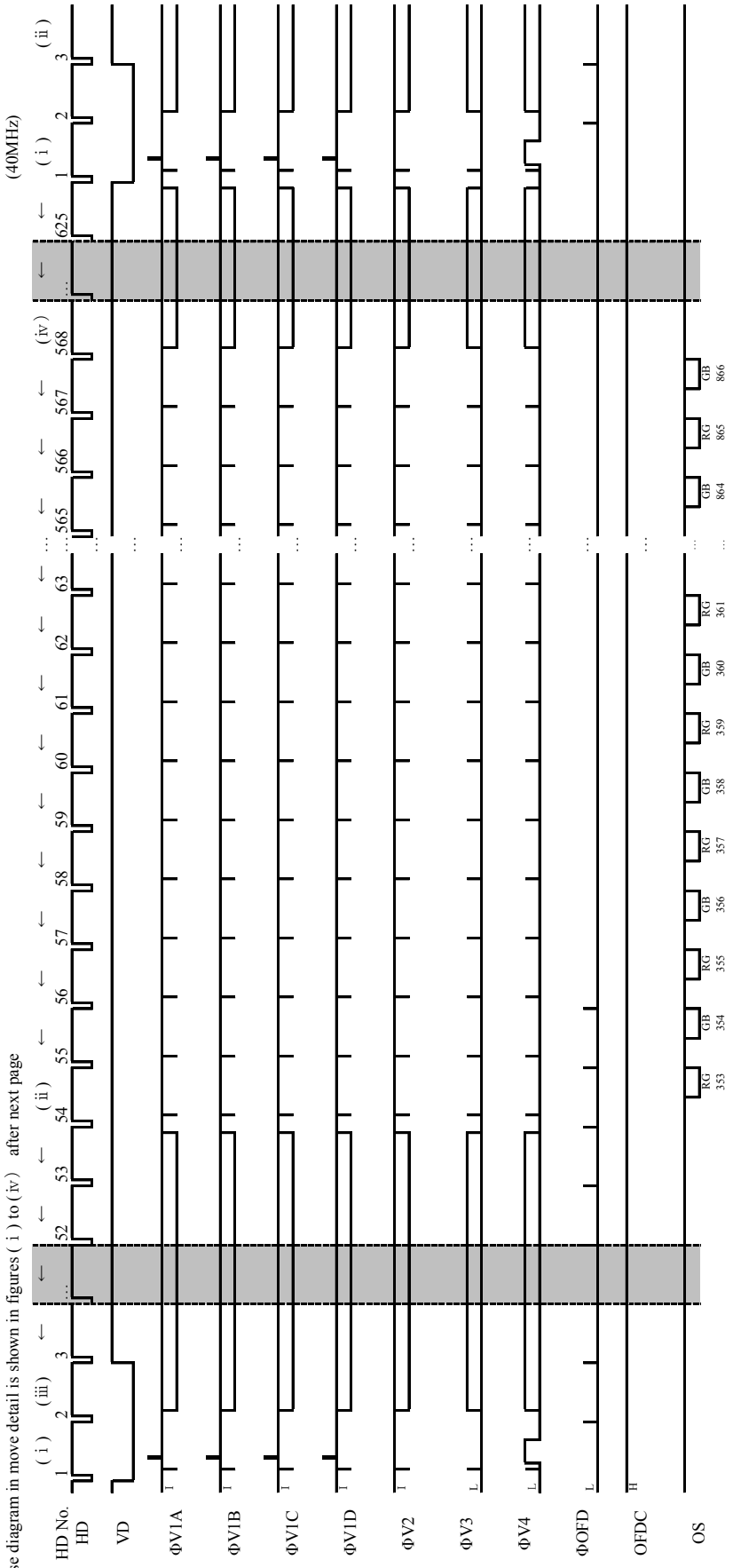


* Keep over the periods indicated in this timing chart when vertical transfer clock pulse is overlapping.

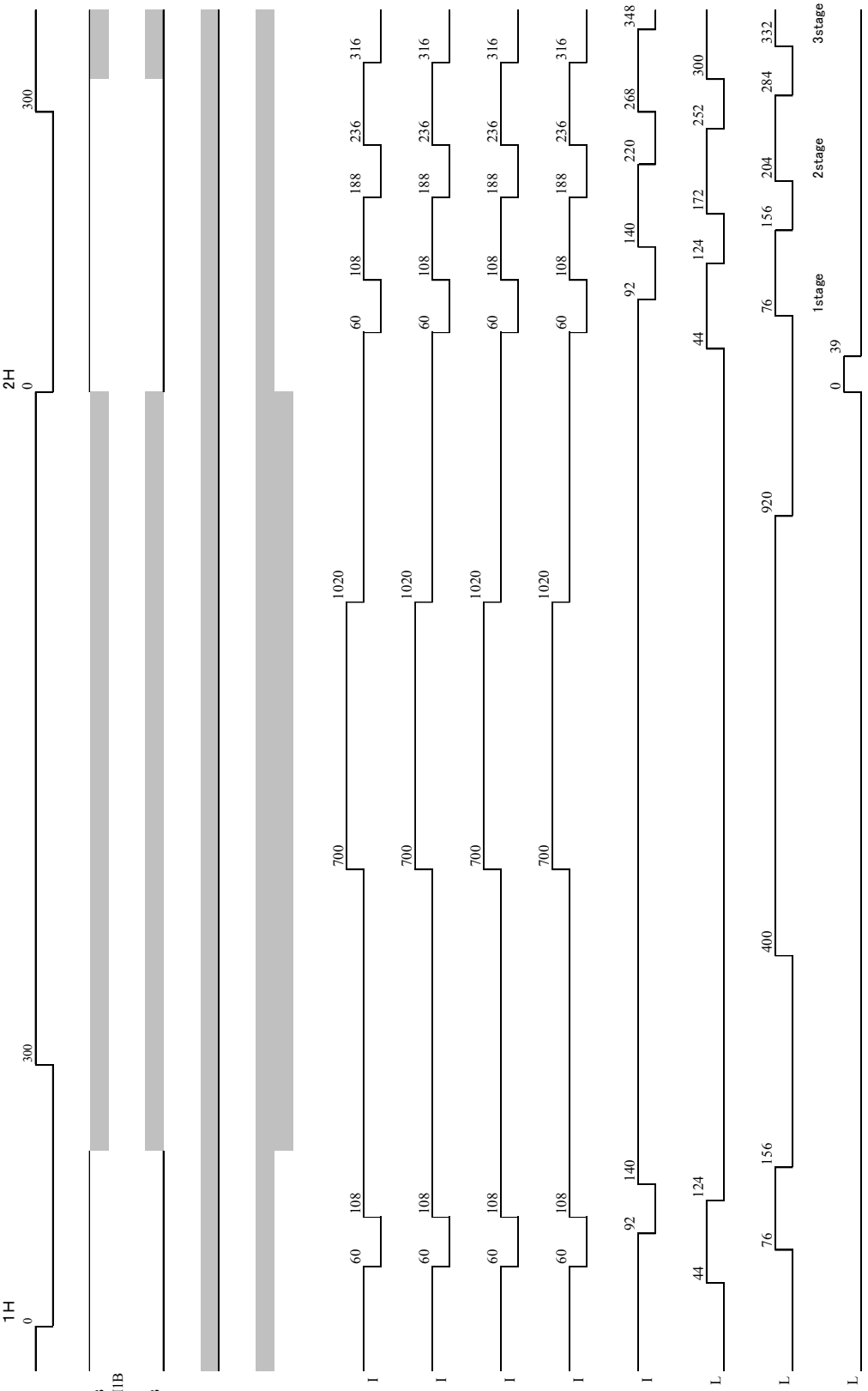
Horizontal transfer timing 【All-pixel readout mode】 fck=40MHz 29.97fps (ii)



Vertical transfer timing【Progressive scan mode[Center 514 line]】fck=40MHz 60fps

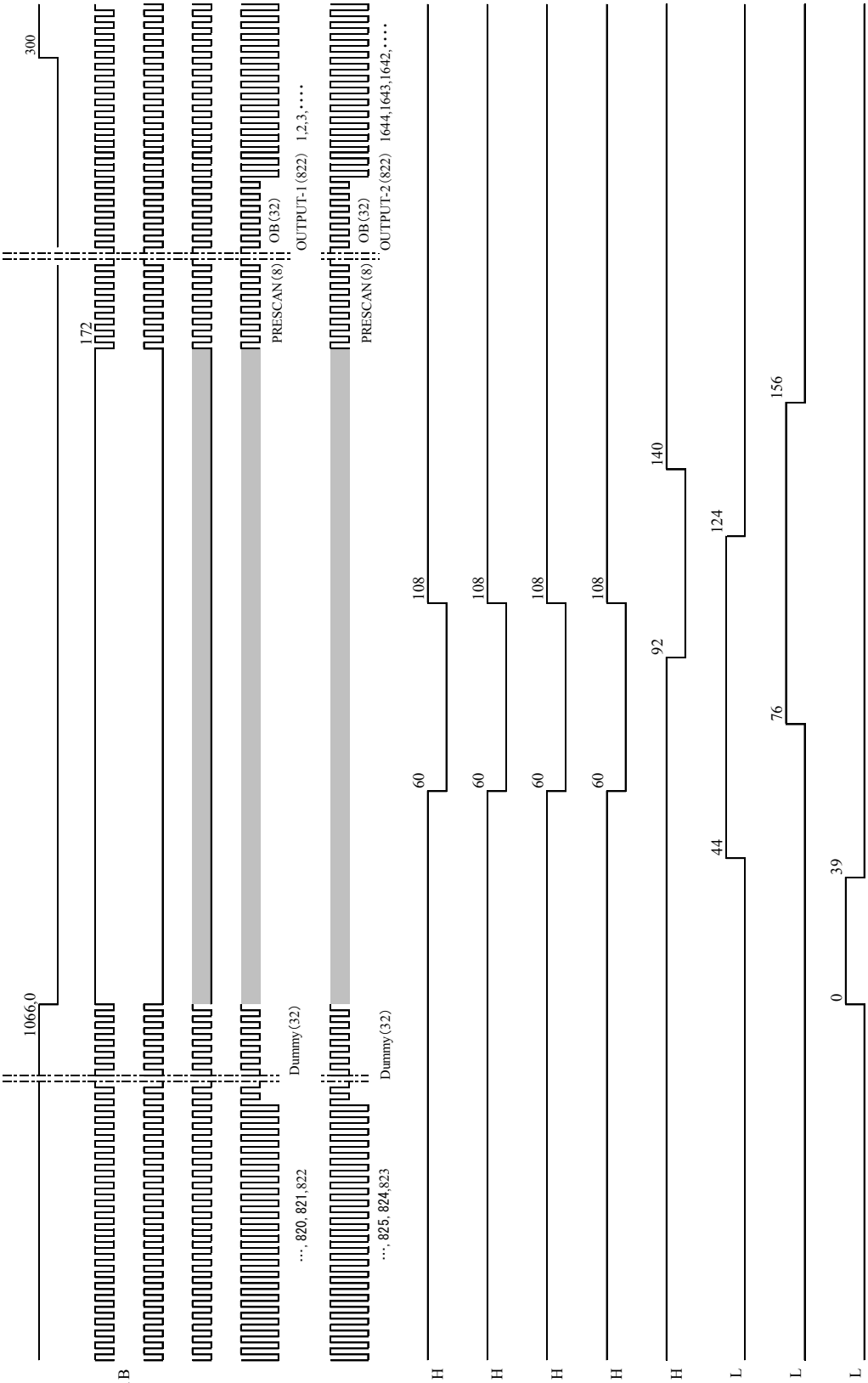


Readout timing【Progressive scan mode[Center 514 line]】fck=40MHz 60fps（i）



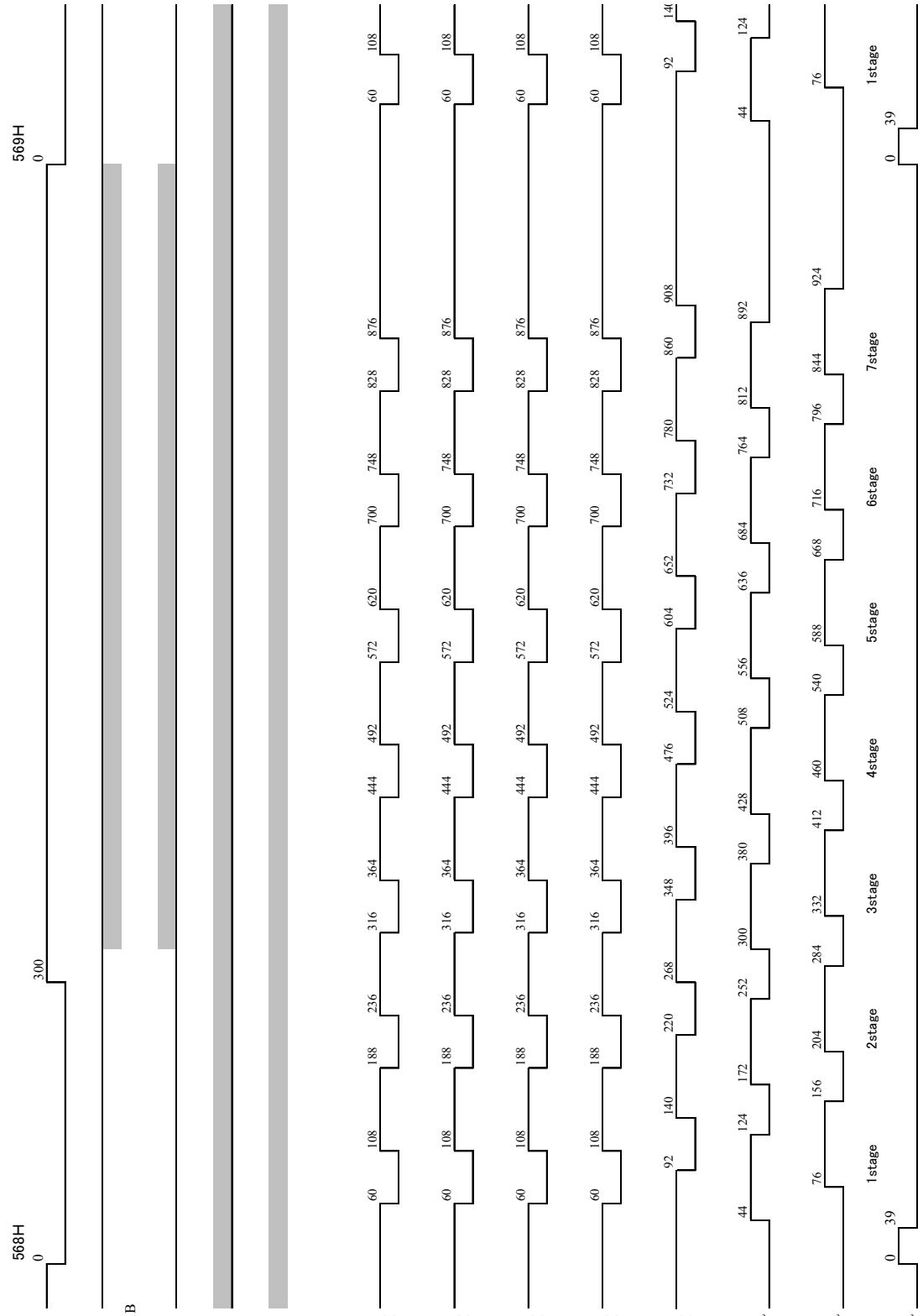
* Keep over the periods indicated in this timing chart when vertical transfer clock pulse is overlapping.

Horizontal transfer timing【Progressive scan mode[Center 514 line]】fck=40MHz 60fps（ii）



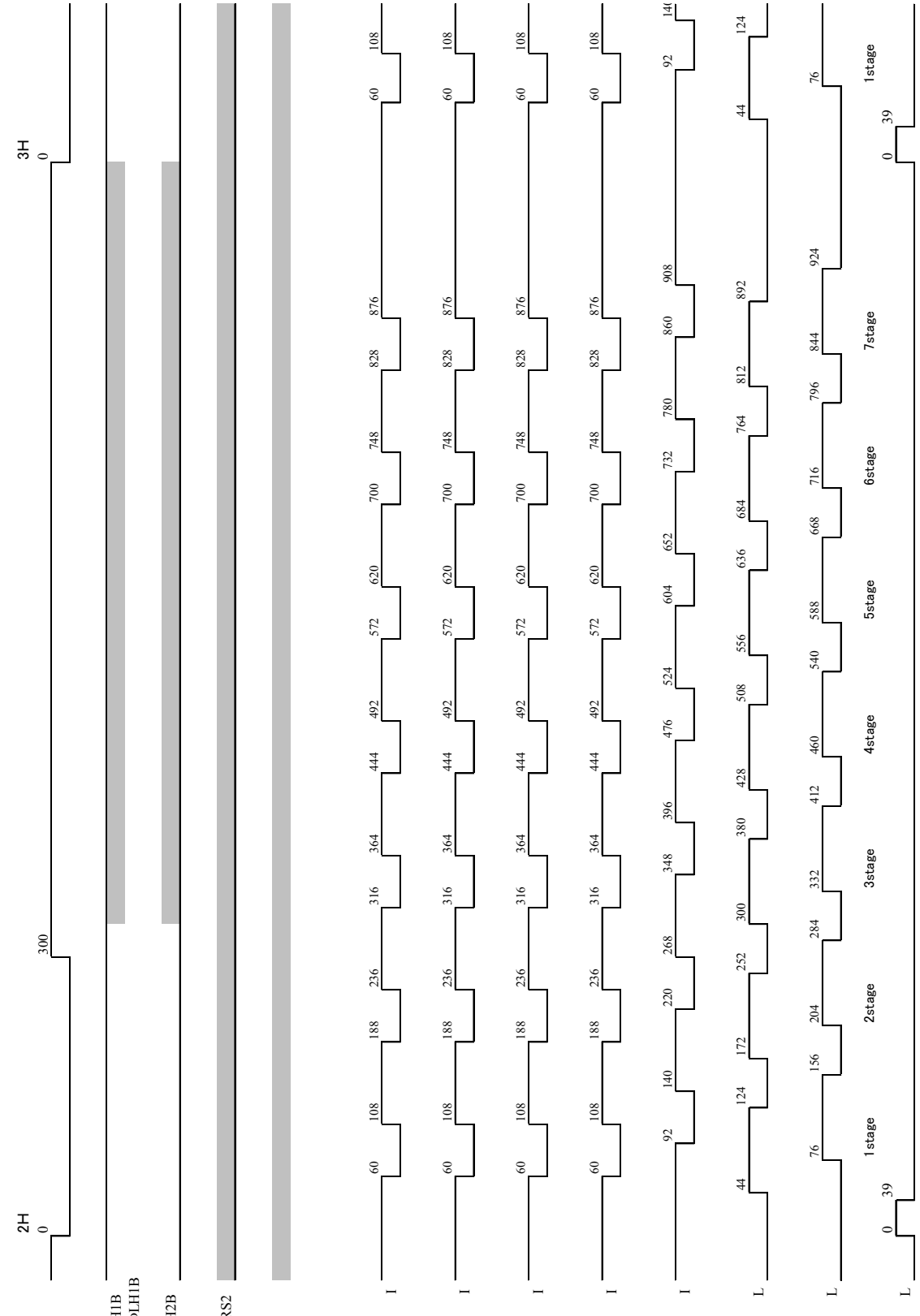
* Keep over the periods indicated in this timing chart when vertical transfer clock pulse is overlapping.

Fast shift transfer timing【Progressive scan mode[Center 514 line]】fck=40MHz 60fps (iii)



* Keep over the periods indicated in this timing chart when vertical transfer clock pulse is overlapping.

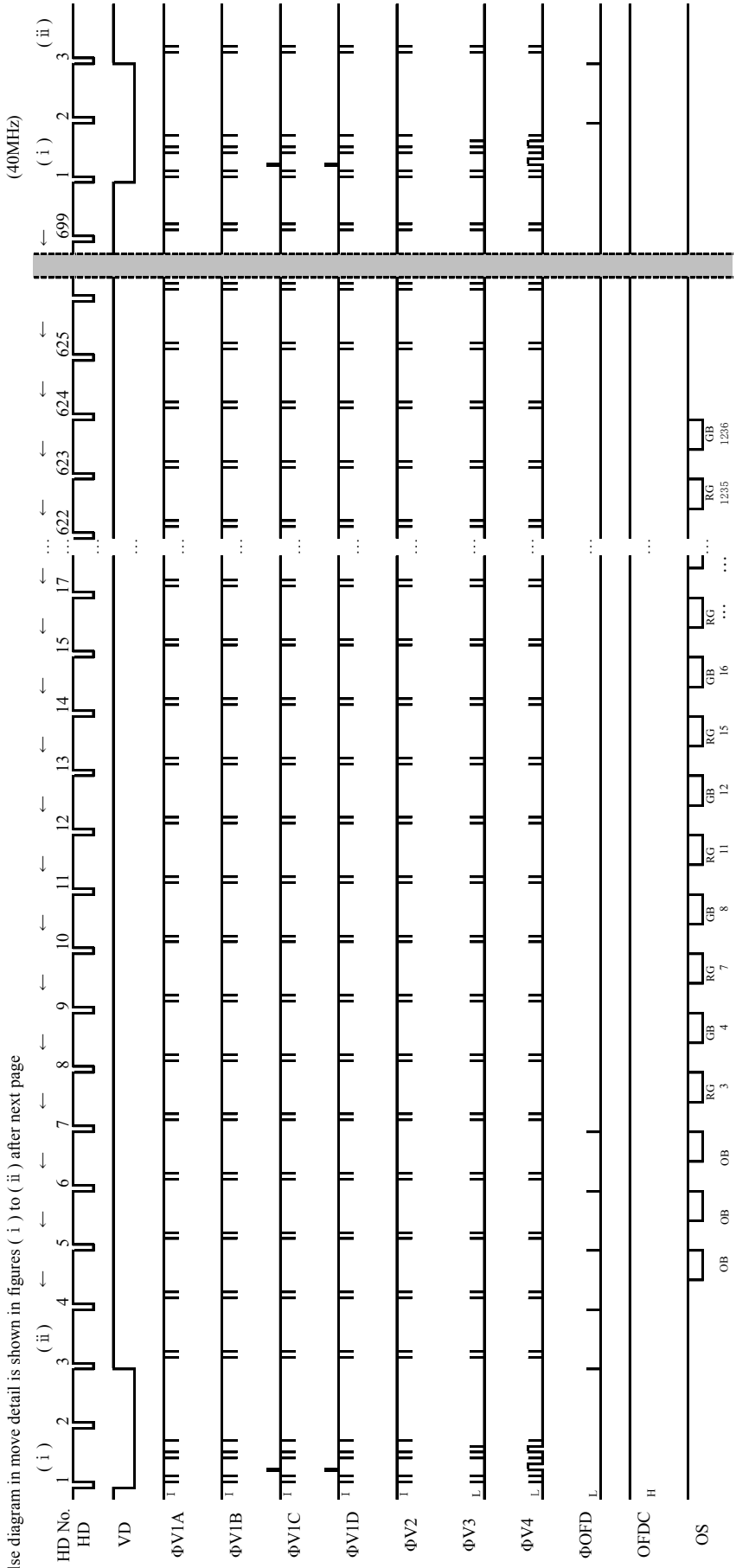
Charge swept transfer timing【 Progressive scan mode[Center 514 line] 】 fck=40MHz 60fps（iv）



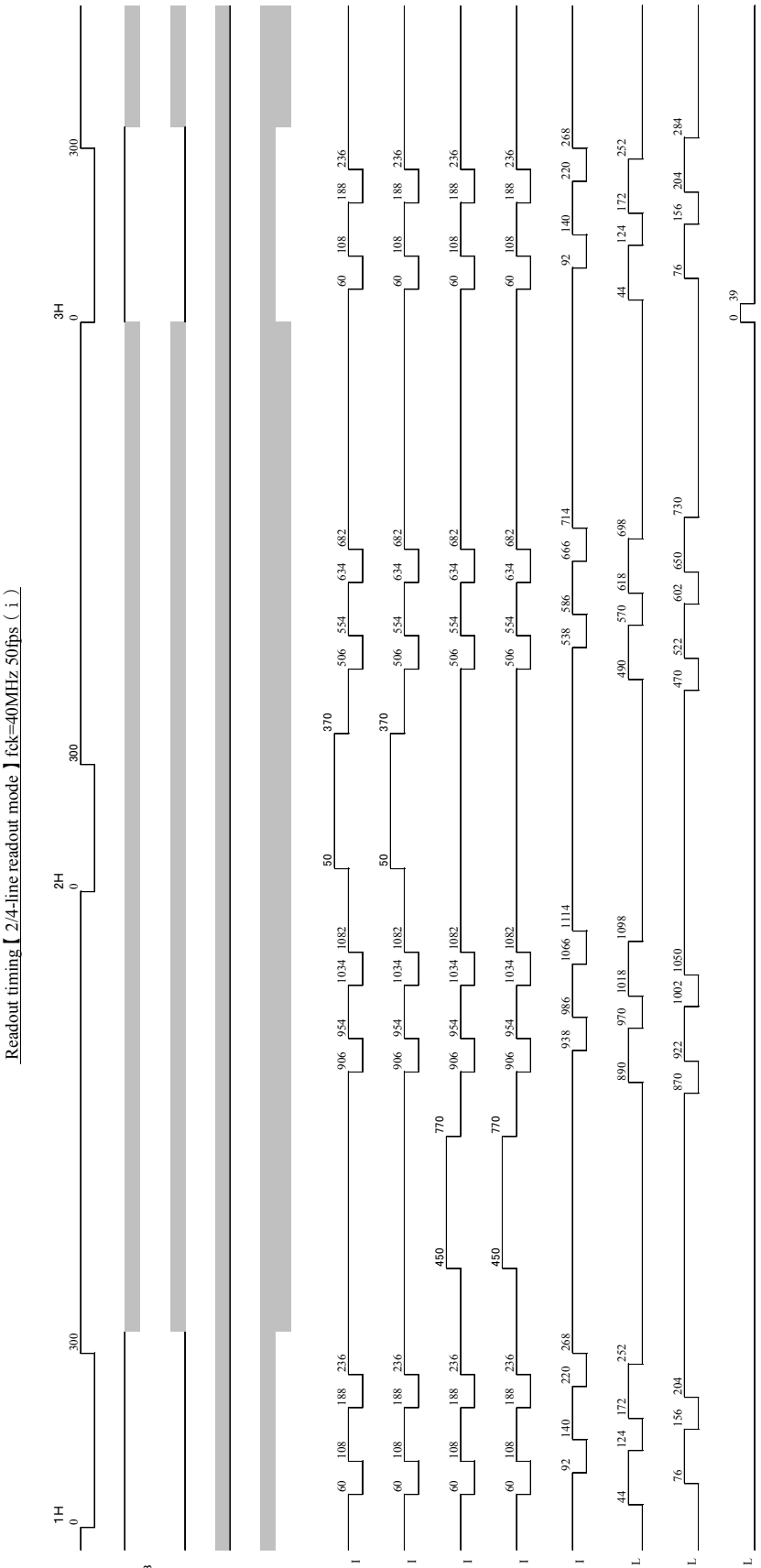
* Keep over the periods indicated in this timing chart when vertical transfer clock pulse is overlapping.

Vertical transfer timing【 2/4-line readout mode 】fck=40MHz 50fps

Pulse diagram in move detail is shown in figures (i) to (ii) after next page

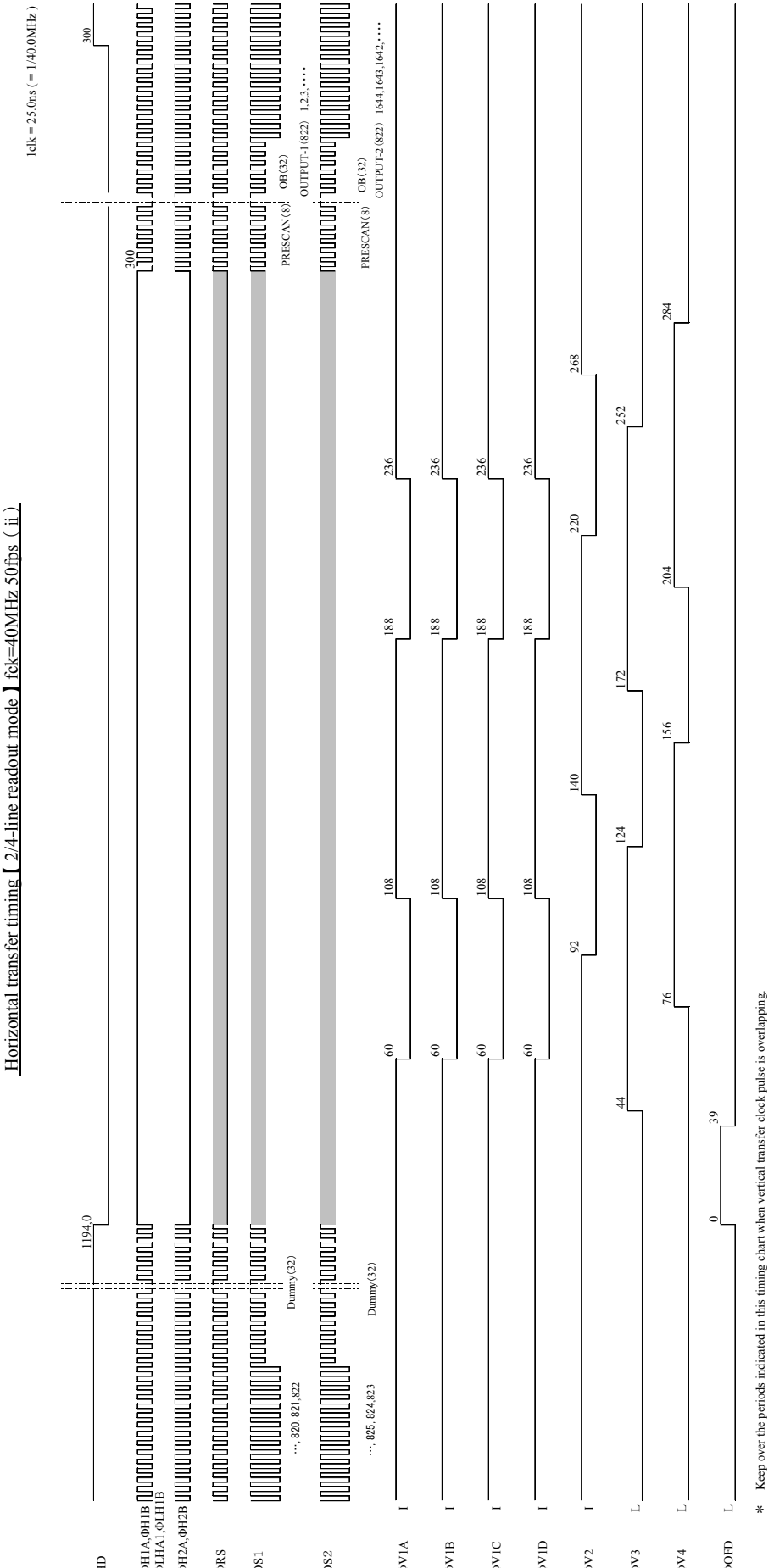


Readout timing【2/4-line readout mode】fck=40MHz 50fps（i）



* Keep over the periods indicated in this timing chart when vertical transfer clock pulse is overlapping.

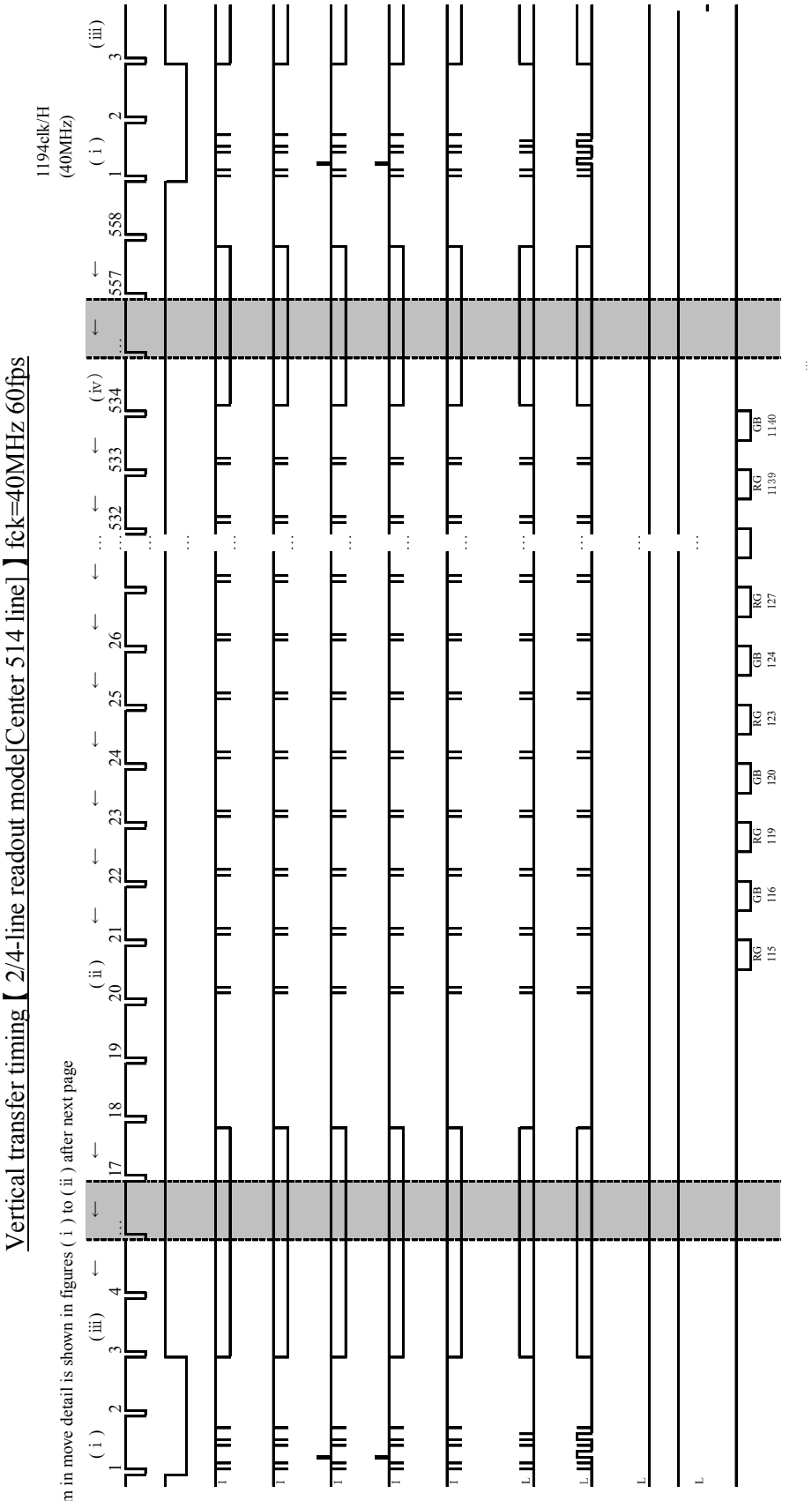
Horizontal transfer timing【2/4-line readout mode】fck=40MHz 50fps（ii）



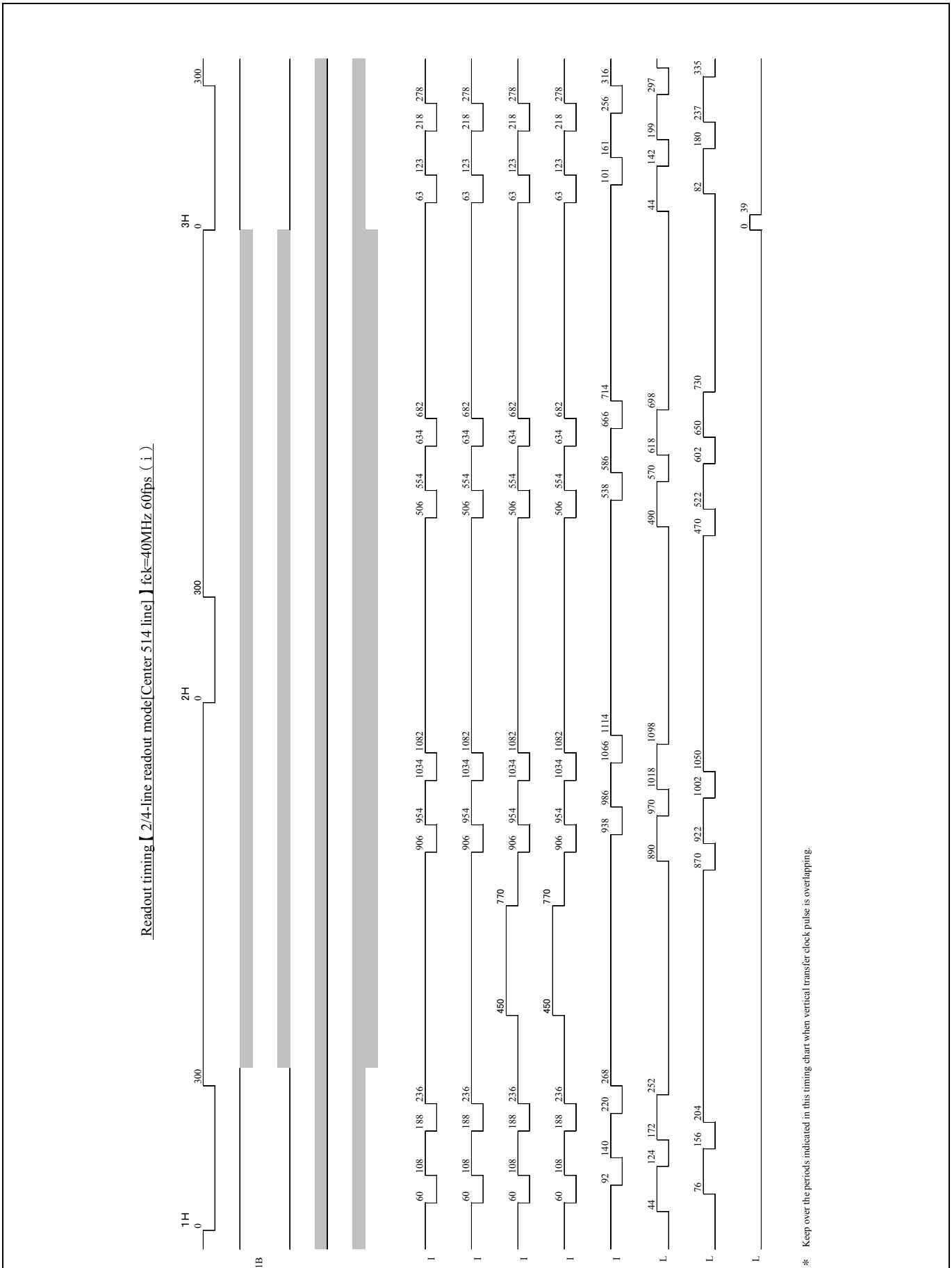
* Keep over the periods indicated in this timing chart when vertical transfer clock pulse is overlapping.

Vertical transfer timing【2/4-line readout mode[Center 514 line]】fck=40MHz 60fps

Pulse diagram in move detail is shown in figures (i) to (ii) after next page

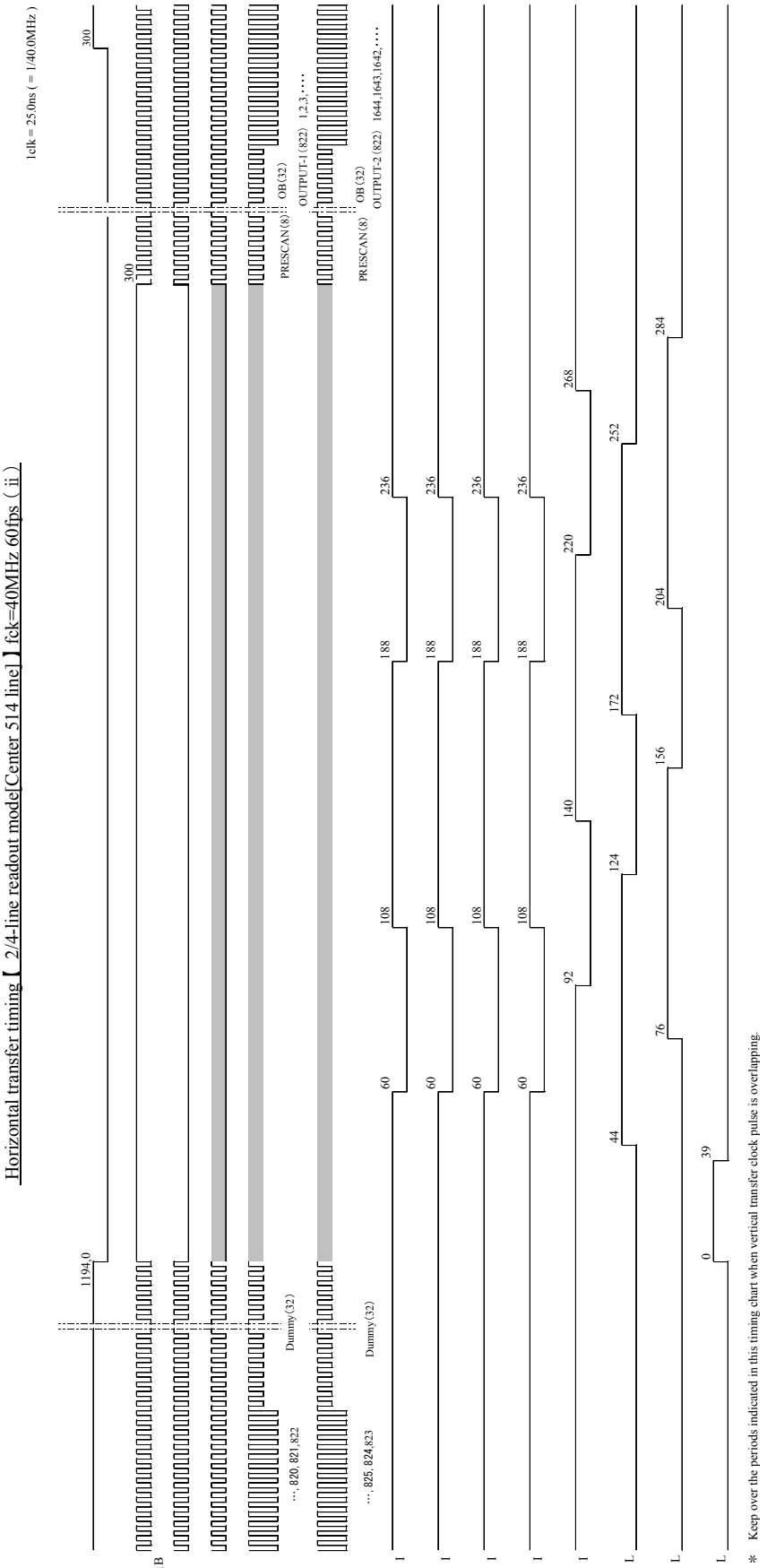


Readout timing【2/4-line readout mode[Center 514 line】fck=40MHz 60fps（i）



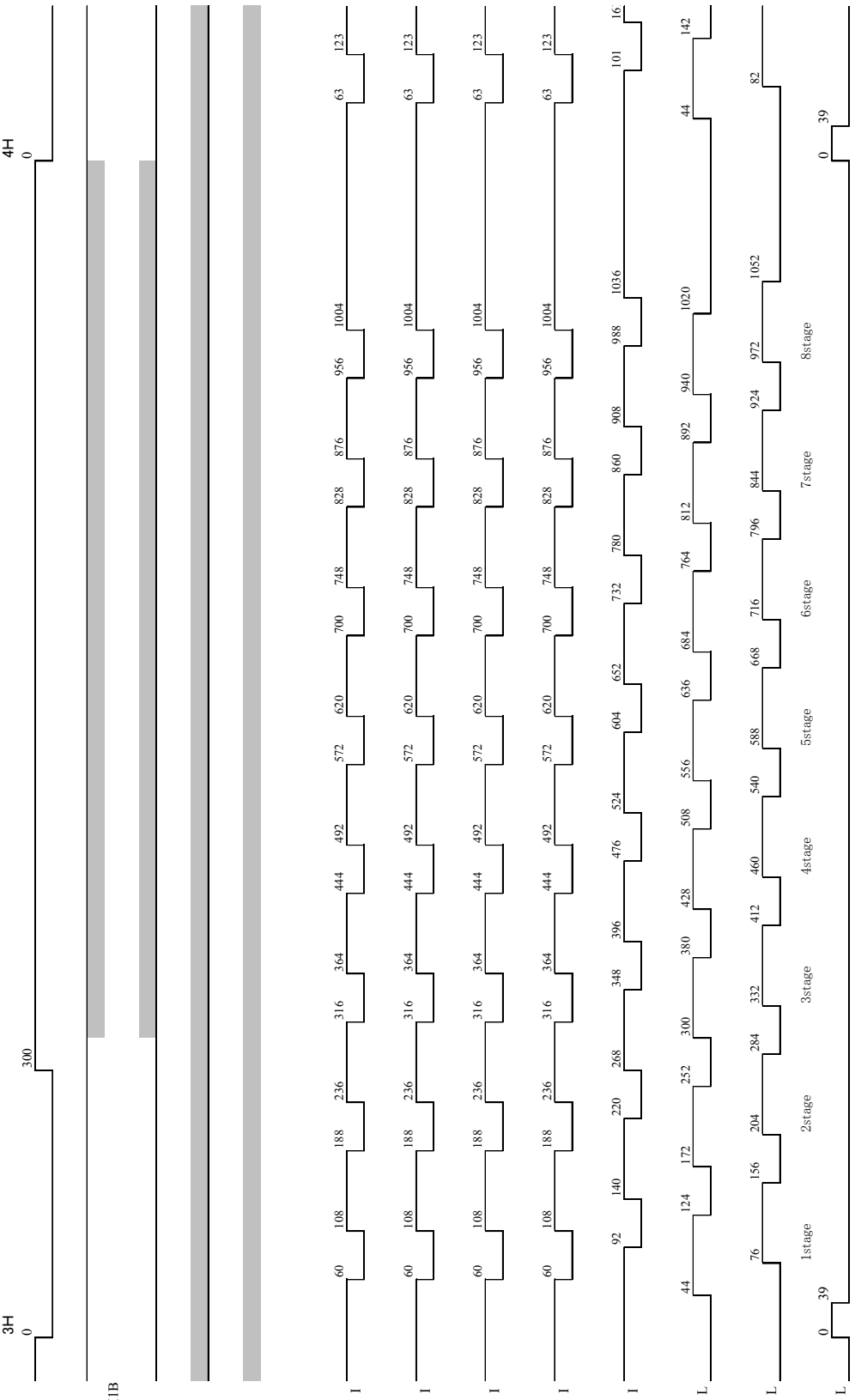
* Keep over the periods indicated in this timing chart when vertical transfer clock pulse is overlapping.

Horizontal transfer timing【2/4-line readout mode[Center 514 line]】fck=40MHz 60fps（ii）



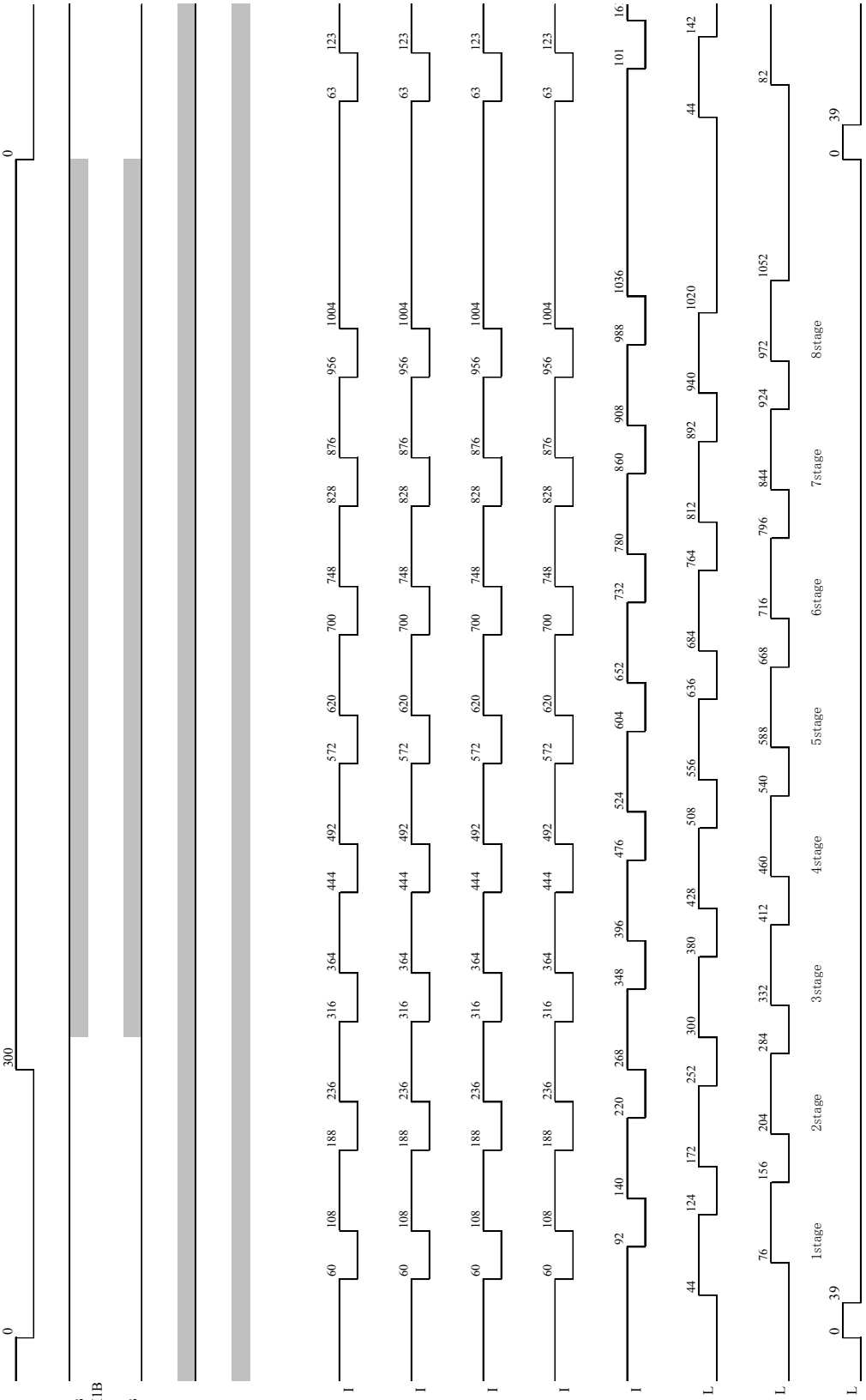
* Keep over the periods indicated in this timing chart when vertical transfer clock pulse is overlapping.

Fast shift transfer timing【2/4-line readout mode[Center 514 line】fck=40MHz 60fps（iii）



＊ Keep over the periods indicated in this timing chart when vertical transfer clock pulse is overlapping.

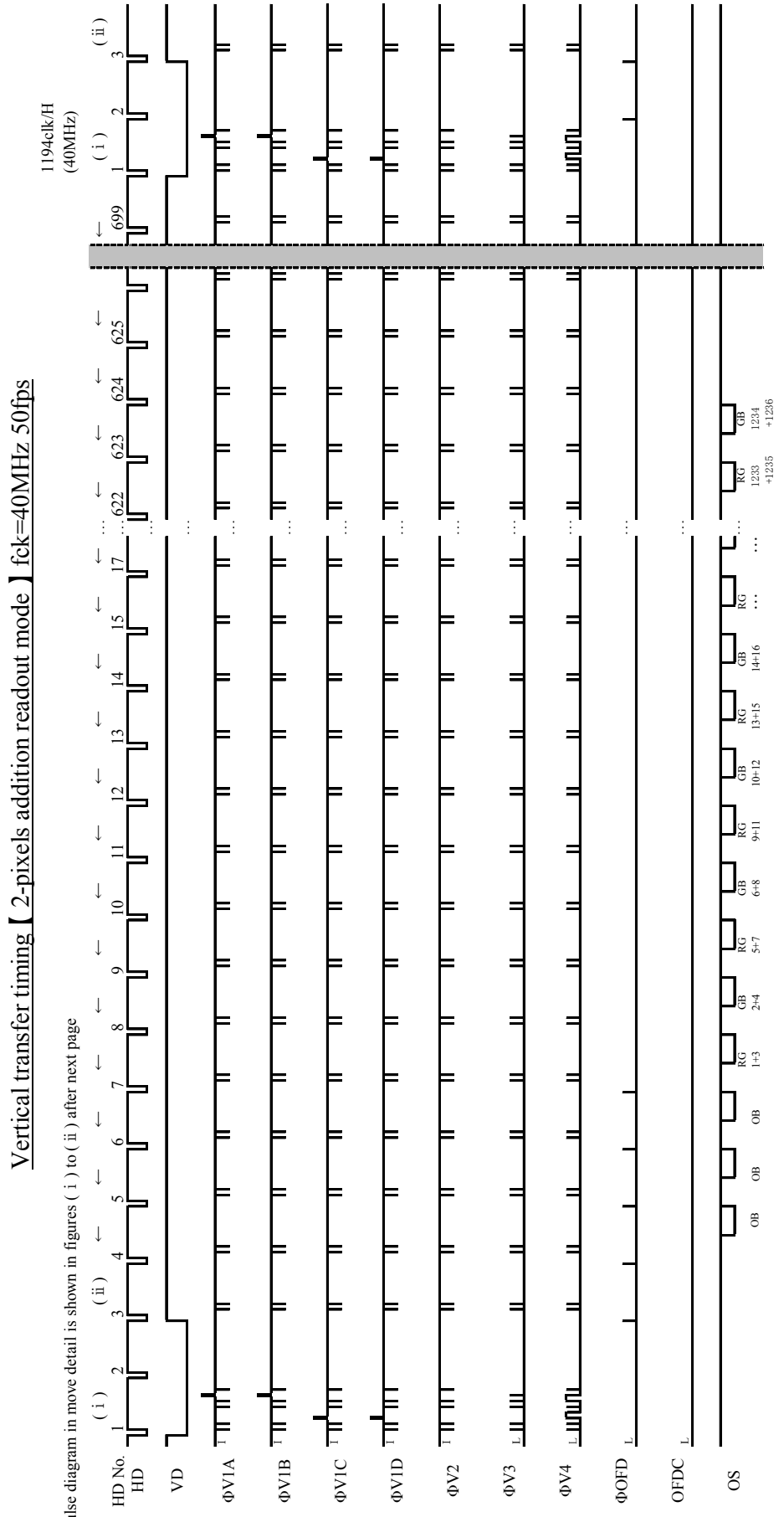
Charge swept transfer timing【2/4-line readout mode[Center 514 line】fck=40MHz 60fps（iv）



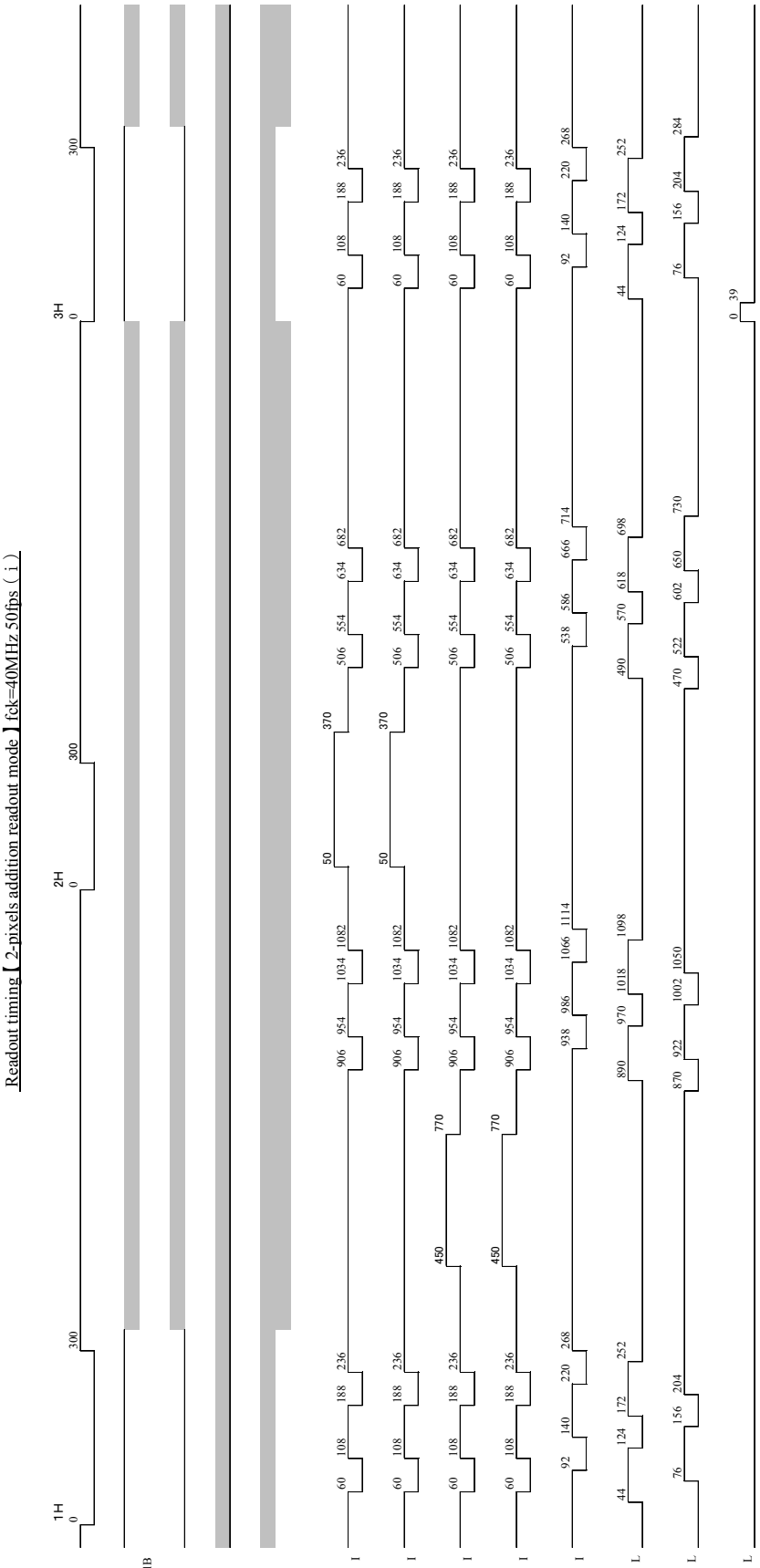
＊ Keep over the periods indicated in this timing chart when vertical transfer clock pulse is overlapping.

Vertical transfer timing【2-pixels addition readout mode】fck=40MHz 50fps

Pulse diagram in move detail is shown in figures (i) to (ii) after next page

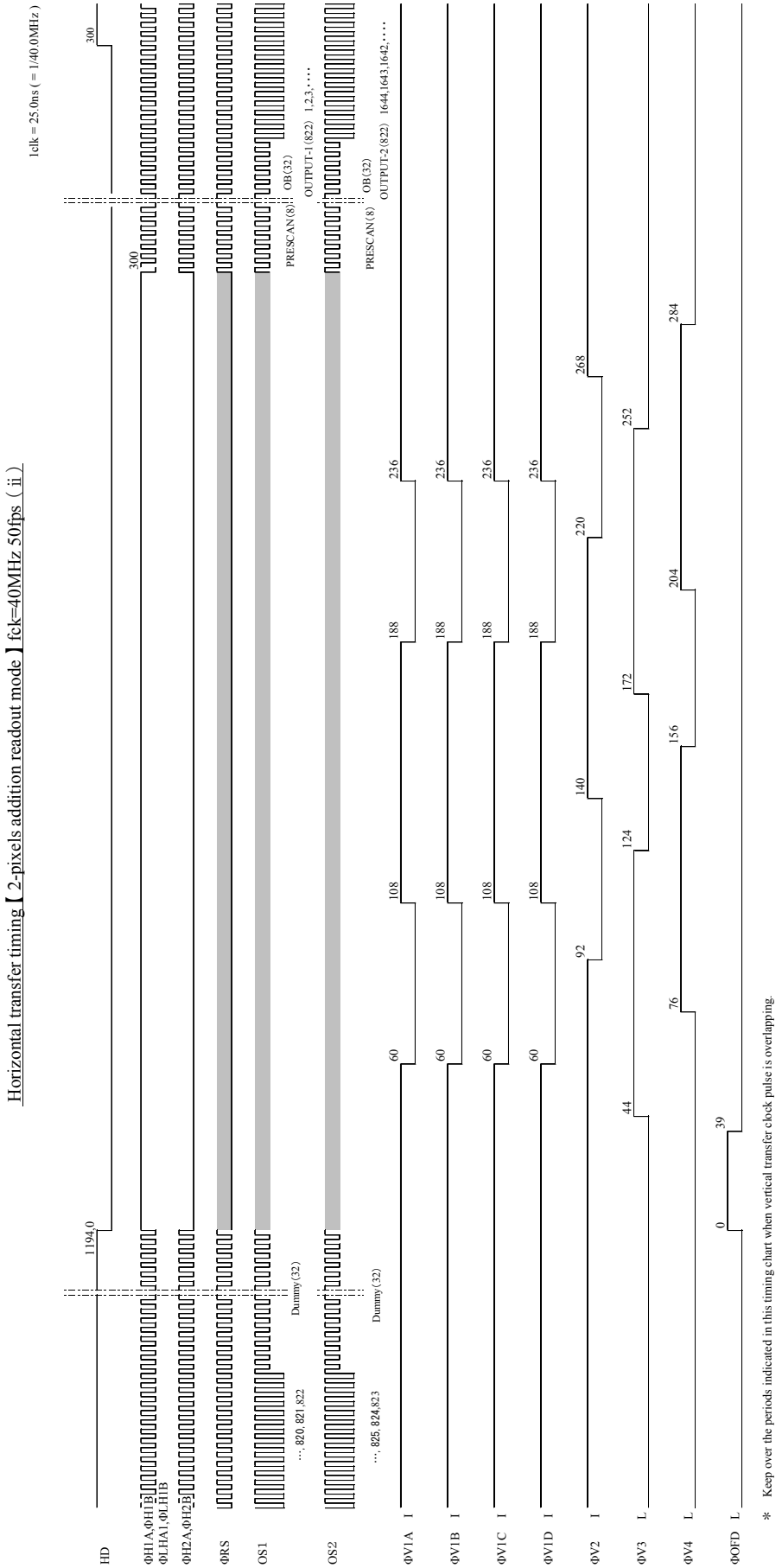


Readout timing【2-pixels addition readout mode】fck=40MHz 50fps（i）



* Keep over the periods indicated in this timing chart when vertical transfer clock pulse is overlapping.

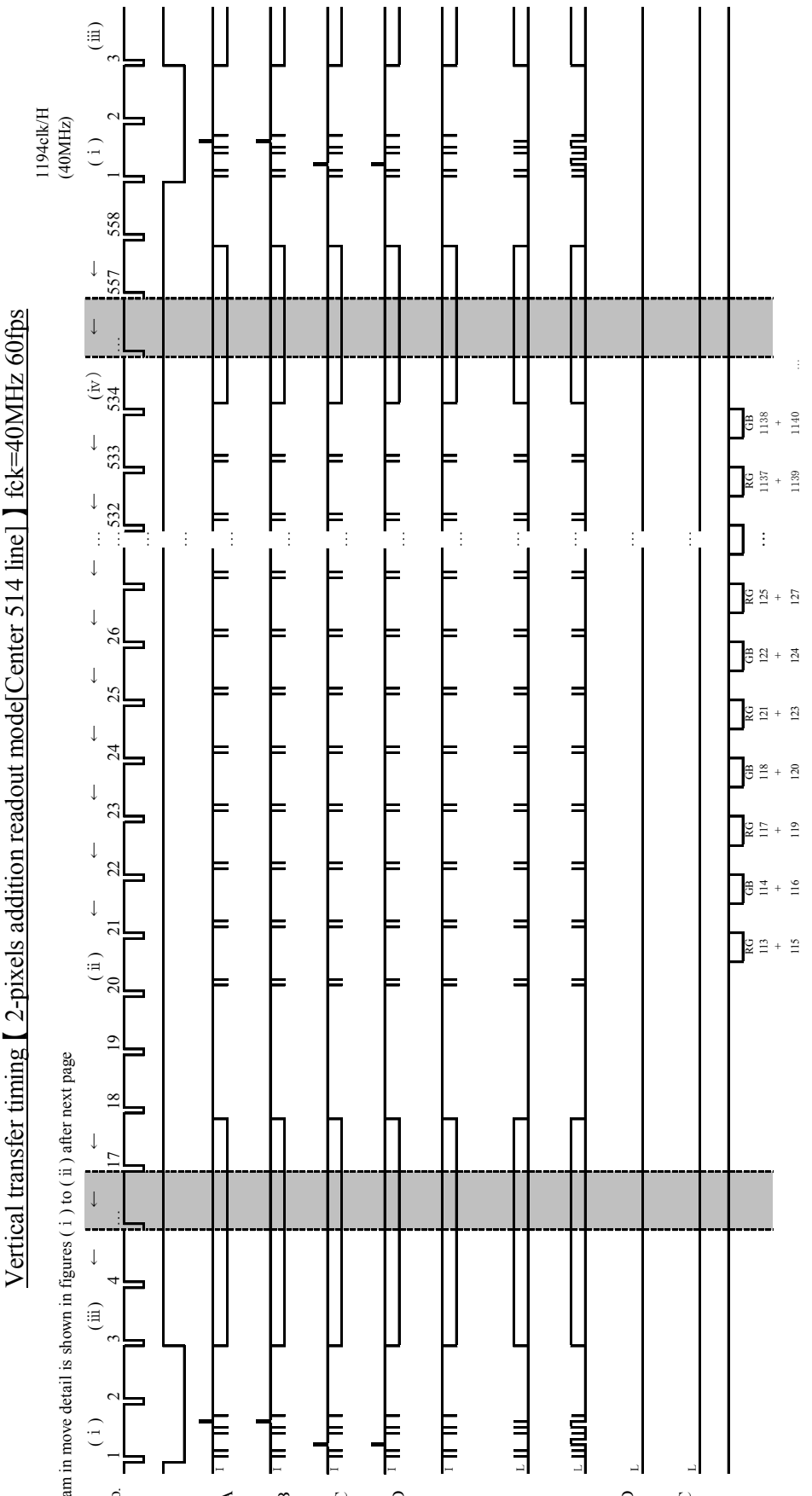
Horizontal transfer timing【2-pixels addition readout mode】fck=40MHz 50fps（ii）



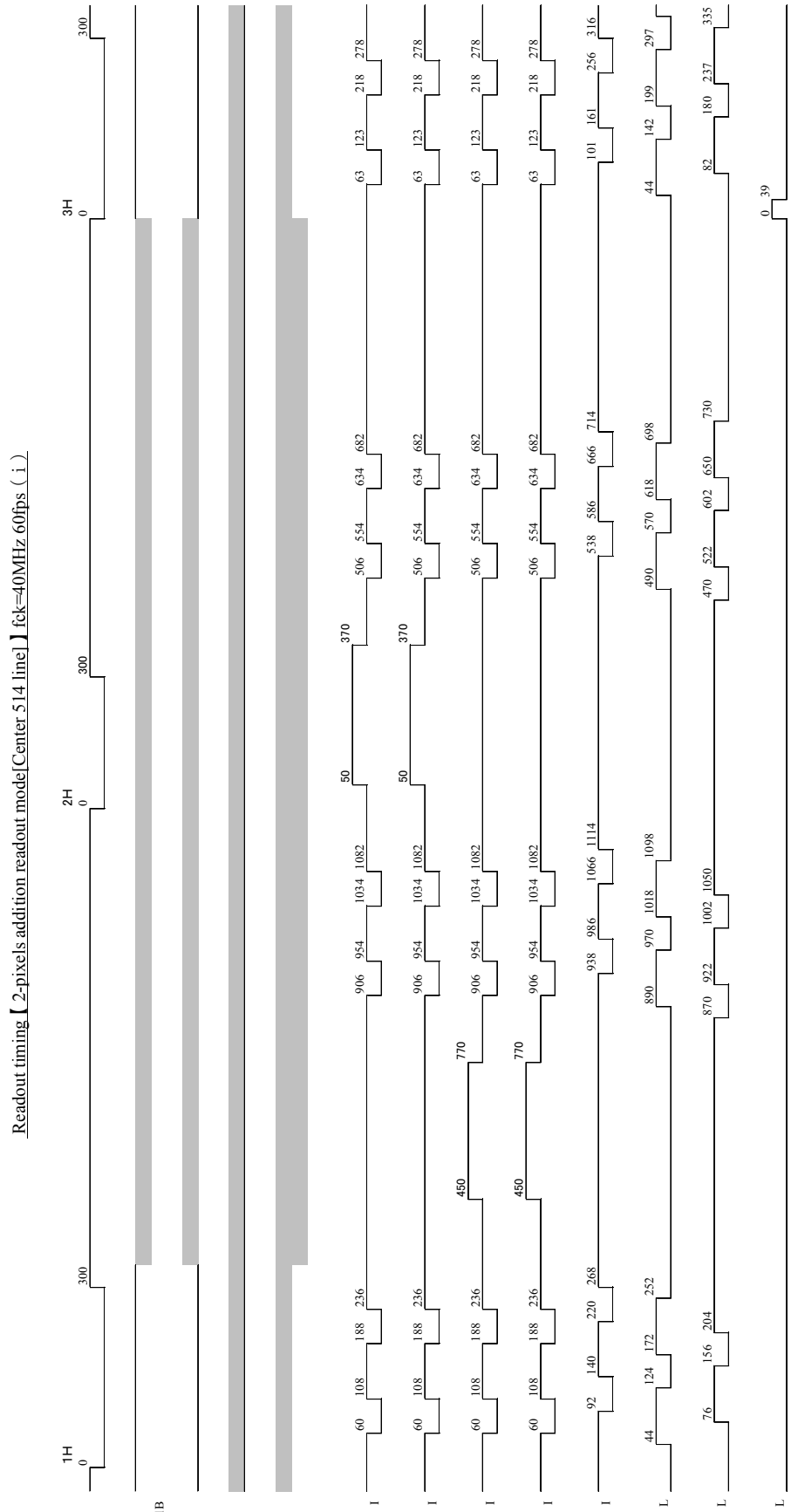
＊ Keep over the periods indicated in this timing chart when vertical transfer clock pulse is overlapping.

Vertical transfer timing【2-pixels addition readout mode[Center 514 line]】fck=40MHz 60fps

Pulse diagram in move detail is shown in figures (i) to (ii) after next page

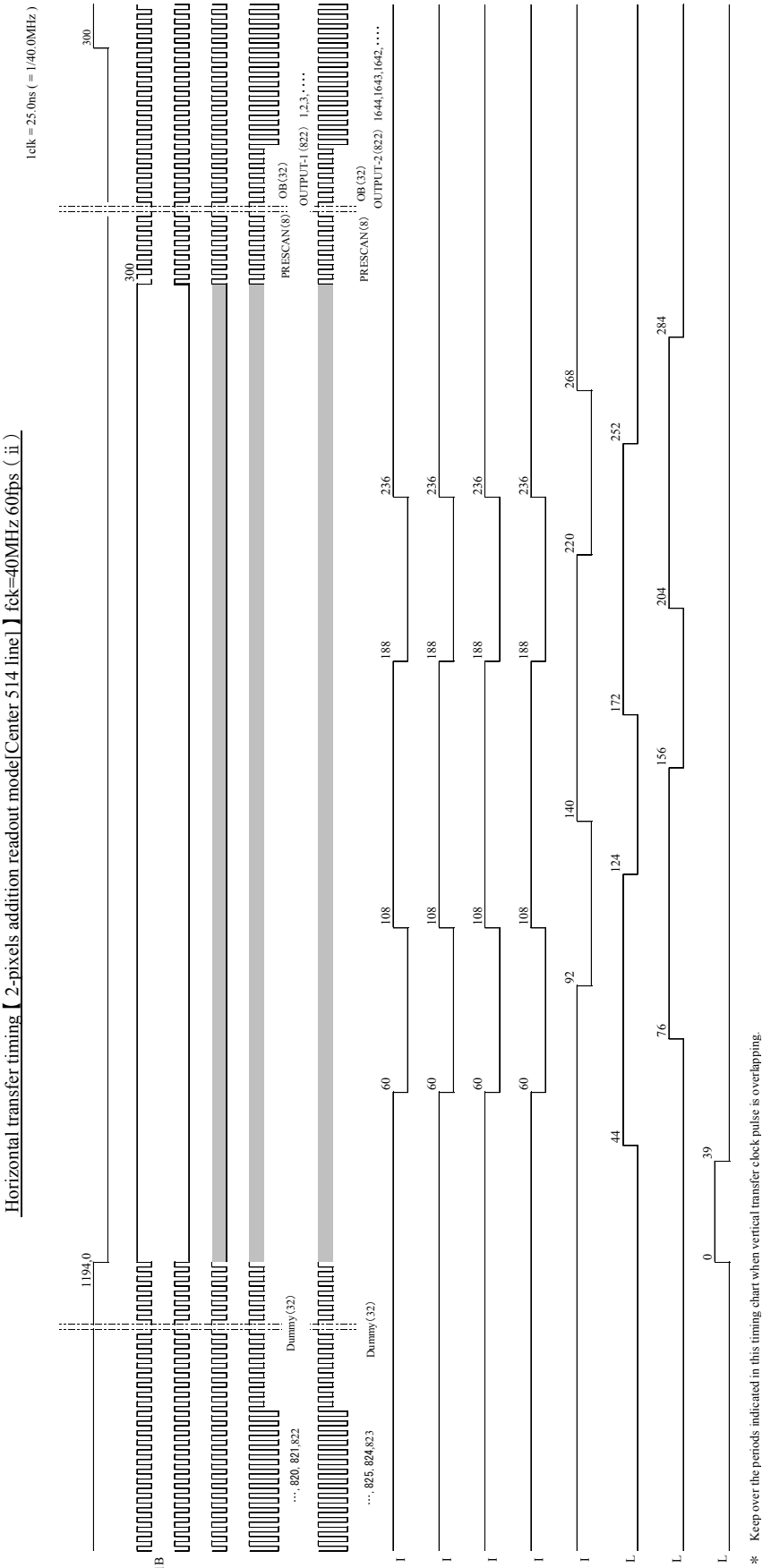


Readout timing【2-pixels addition readout mode[Center 514 line]】fck=40MHz 60fps（i）

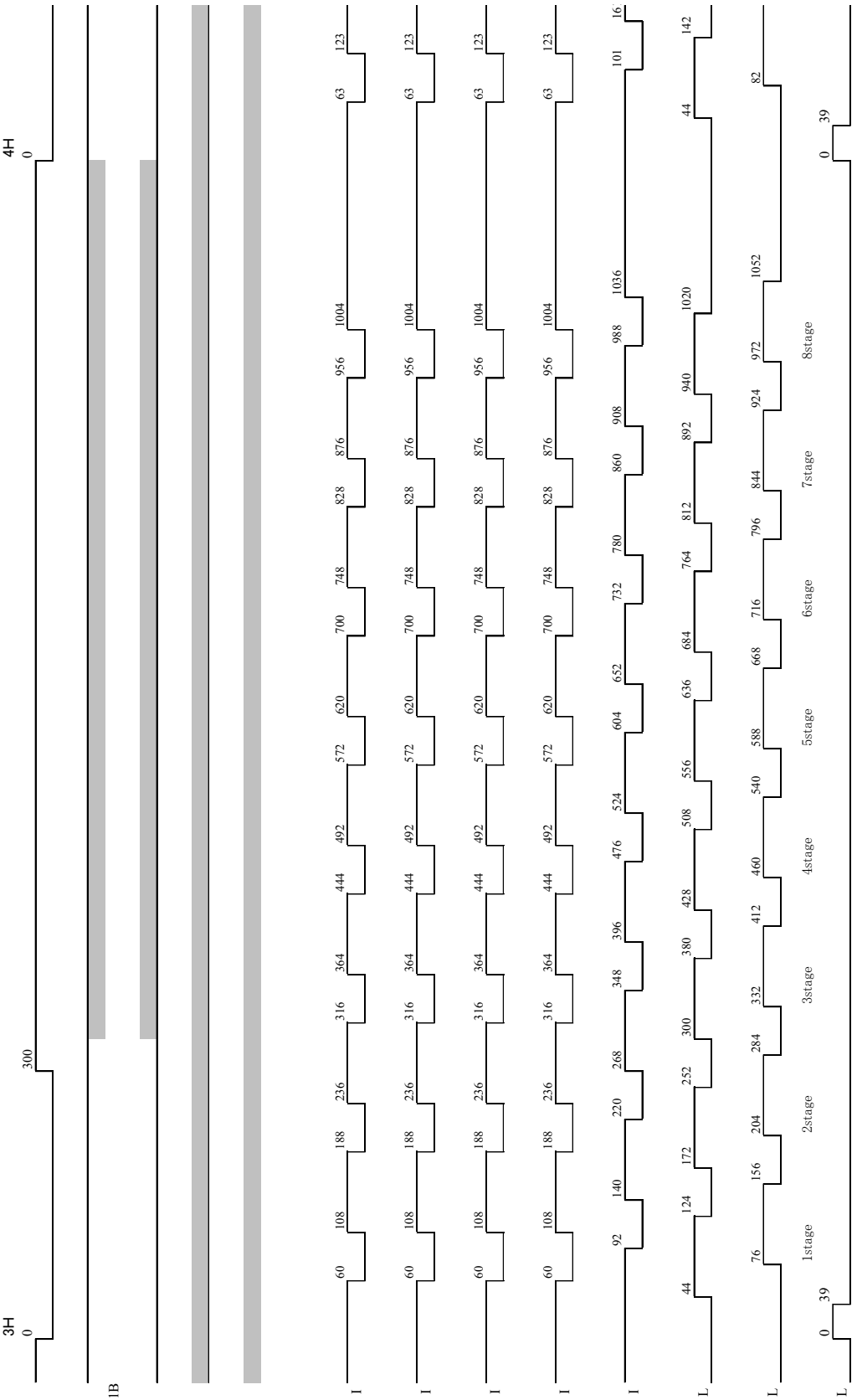


* Keep over the periods indicated in this timing chart when vertical transfer clock pulse is overlapping.

Horizontal transfer timing【2-pixels addition readout mode[Center 514 line]】fck=40MHz 60fps（ii）

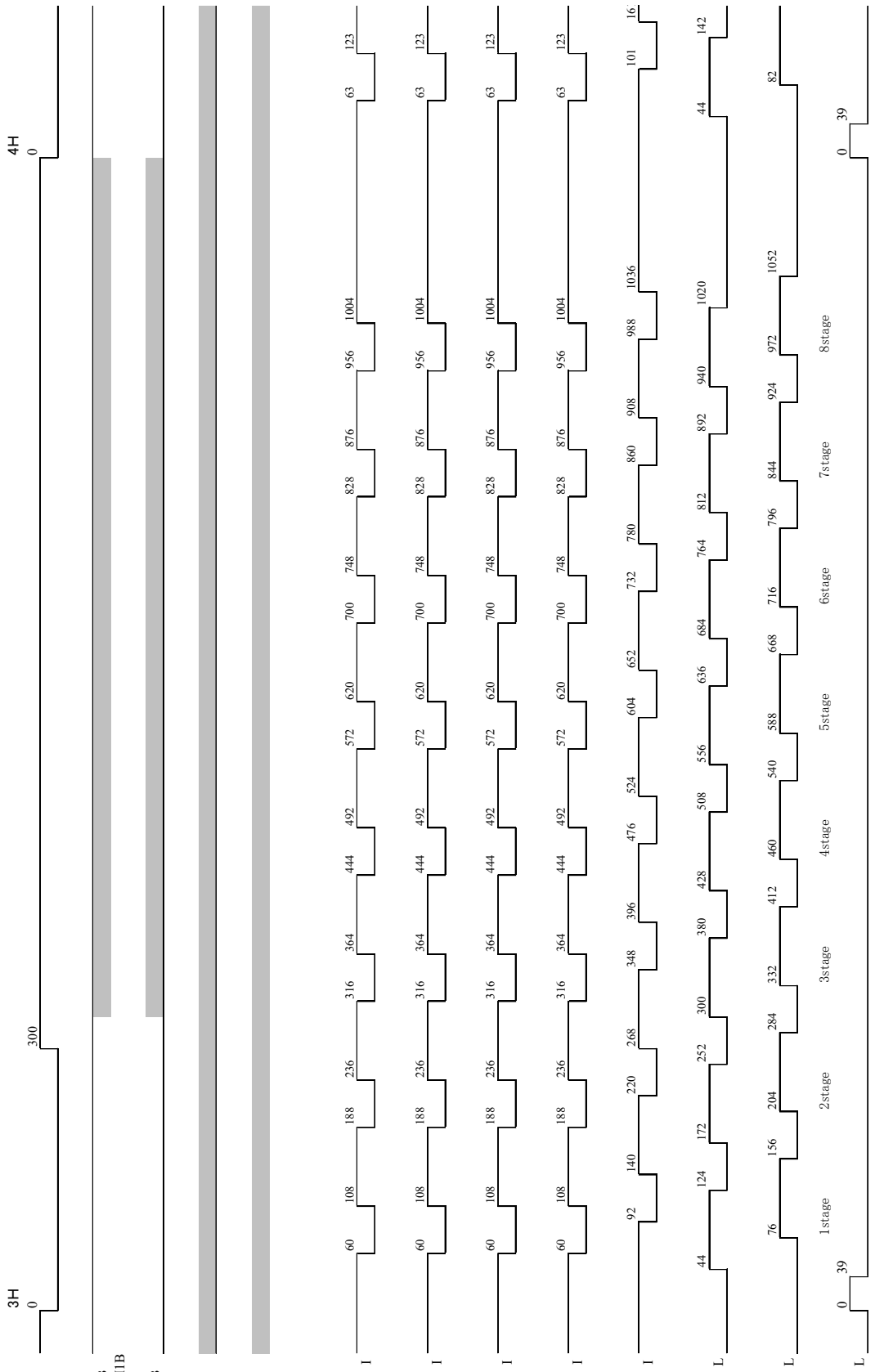


Fast shift transfer timing【2-pixels addition readout mode[Center 514 line]】fck=40MHz 60fps（iii）



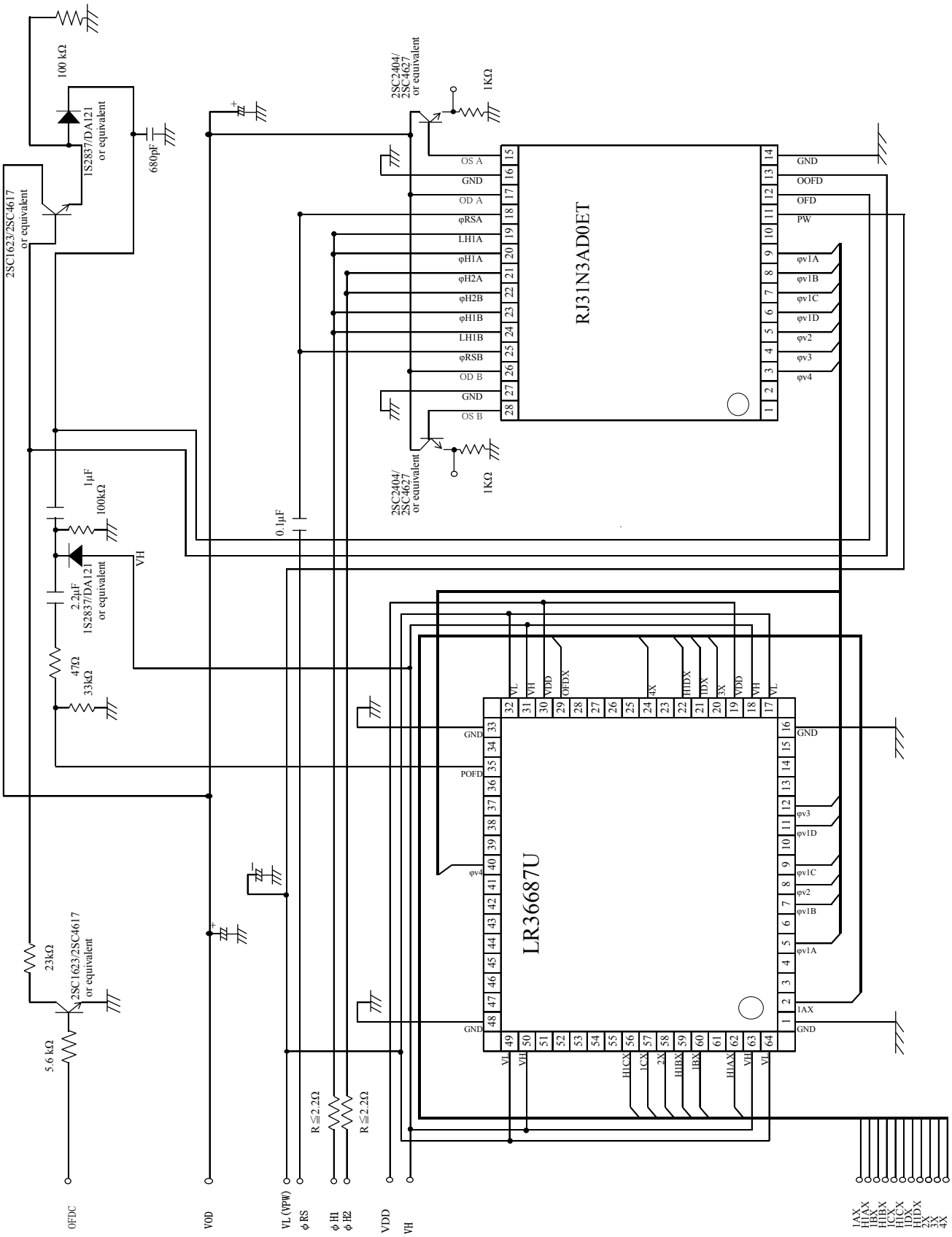
* Keep over the periods indicated in this timing chart when vertical transfer clock pulse is overlapping.

Charge swept transfer timing【2-pixels addition readout mode[Center 514 line]】fck=40MHz 60fps（iv）



* Keep over the periods indicated in this timing chart when vertical transfer clock pulse is overlapping.

8 EXAMPLE OF STANDARD OPERATING CIRCUIT



9 SPECIFICATION FOR BLEMISH (1/30 s frame accumulation)

1) Definition of blemish

	Level of blemish (mV)	Permitted number of blemish	Comment
White blemish (Exposed)	50 ≦ B	0	・See fig.9-1(a), fig.9-2. ・Vout = Vstd
	B < 50	no count	
Black blemish (Exposed)	120≦ B	0	
	55≦ B <120	10	
	40≦ B < 55	10	
	B < 40	no count	
White blemish (Non-Exposed)	100< B	0	・See fig.9-1(b), fig.9-2 ・N≦60 ・M+N≦300
	20< B ≦100	N	
	2.5< B ≦ 20	M	
	B ≦2.5	no count	
White blemish (Shutter mode)	5.0≦ B	0	・See fig.9-1(a), fig.9-2. ・Vout = Vstd/10 ・The electronic shutter speed is set at 1/10000 s
	B <5.0	no count	
Black blemish (Shutter mode)	5.0≦ B	0	
	B <5.0	no count	

＊Total number of white blemish (non-exposed:20< B ≦100) and black blemish (exposed: 55≦ B <120)are less than 2 in arbitrary 8×8 pixels areas(ignore color filter).

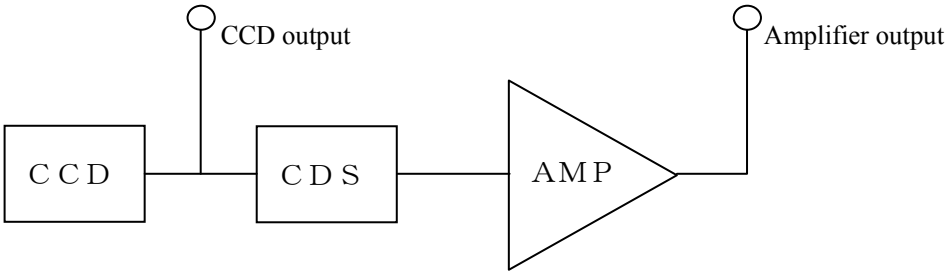
ex. The defects are less than 2 in the subsequent area surrounded b

G	B	G	B	G	B	G	B	G	B
R	G	R	G	R	G	R	G	R	G
G	B	G	B	G	B	G	B	G	B
R	G	R	G	R	G	R	G	R	G
G	B	G	B	G	B	G	B	G	B
R	G	R	G	R	G	R	G	R	G
G	B	G	B	G	B	G	B	G	B
R	G	R	G	R	G	R	G	R	G
G	B	G	B	G	B	G	B	G	B
R	G	R	G	R	G	R	G	R	G

《note》 ・ B : Blemish level defined in fig. 9-1.
・ Vout : Average output voltage
・ Vstd : 150 mV (The average output voltage of G signal). The standard output voltage defined in the specification of the characteristics.

【MEASURING CONDITION】

・Ｔａ ： 60℃
・Measuring block diagram



The output voltage is measured at the CCD output.
The gain of the amplifier is adjusted to the unity between the CCD output and the amplifier output.

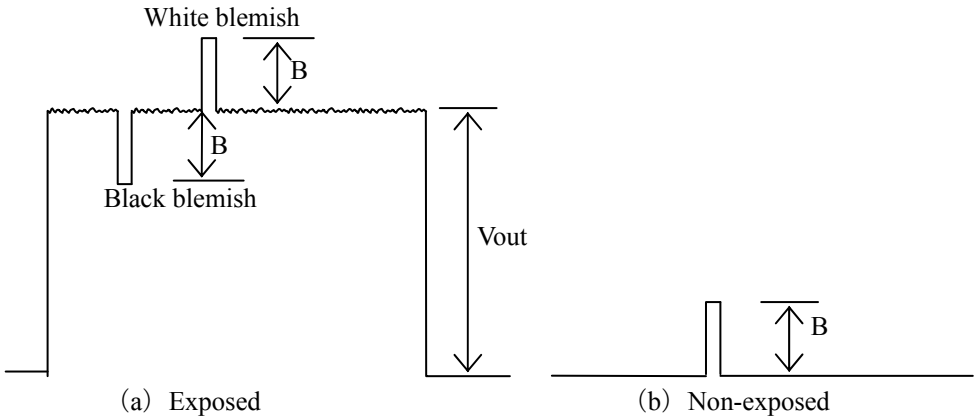


fig. 9-1 Definition of blemish level

(The wave form is the luminance signal measured at the Amplifier output)

【MEASURING AREA】

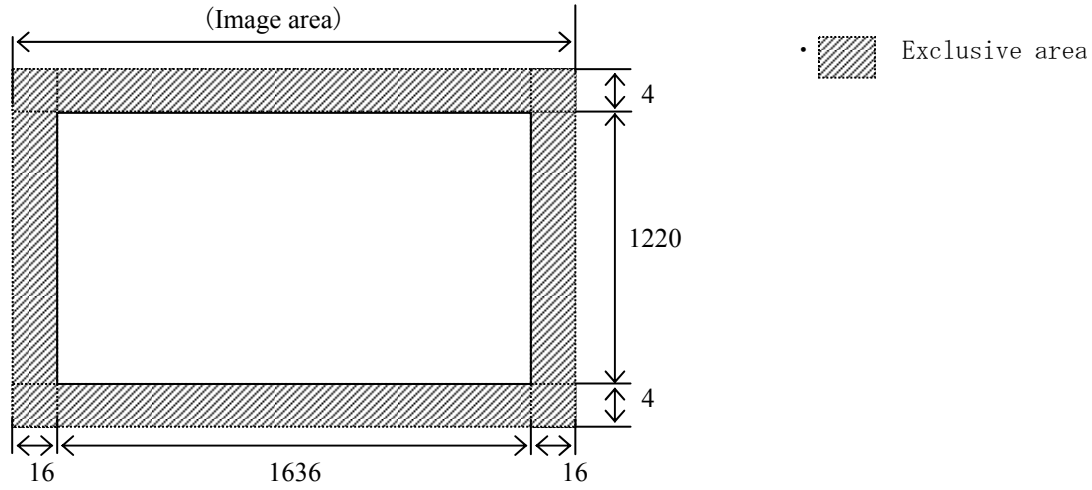


fig. 9-2 Definition of the measuring area

10 PRECAUTIONS

10.1 Package Breakage

In order to prevent the package from being broken, observe the following instructions:

1) The CCD is a precise optical component and the package material is plastic.
Therefore,
- Take care not to drop the device when mounting, handling, or transporting.
- Avoid giving a shock to the package. Especially when leads are fixed to the socket or the circuit board, small shock could break the package more easily than when the package isn't fixed.

2) When mounting the package on the housing, be sure that the package is not bent.
- If a bent package is forced into place between a hard plate or the like, the package may be broken.

3) If any damage or breakage occurs on the surface of the glass cap, its characteristics could deteriorate.
Therefore,
- Do not hit the glass cap.
- Do not give a shock large enough to cause distortion.
- Do not scrub or scratch the glass surface.
- Even a soft cloth or applicator, if dry, could cause flaws to scratch the glass.

10.2 Electrostatic Damage

As compared with general MOS-LSI, CCD has lower ESD.
Therefore, take the following antistatic measures when handling the CCD:

1) Always discharge static electricity by grounding the human body and the instrument to be used.
To ground the human body, provide resistance of about 1 MΩ between the human body and the ground to be on the safe side.
2) When directly handling the device with the fingers, hold the part without leads and do not touch any lead.
3) To avoid generating static electricity,
a. do not scrub the glass surface with cloth or plastic
b. do not attach any tape or labels
c. do not clean the glass surface with dust-cleaning tape
4) When storing or transporting the device, put it in a container of conductive material.

10.3 Dust and Contamination

Dust or contamination on the glass surface could deteriorate the output characteristics or cause a scar. In order to minimize dust or contamination on the glass surface, take the following precautions:

1) Handle the CCD in a clean environment such as a cleaned booth. (The cleanliness level should be, if possible, class 1,000 at least.)

2) Do not touch the glass surface with the fingers. If dust or contamination gets on the glass surface, the following cleaning method is recommended:

- Dust from static electricity should be blown off with an ionized air blower. For anti-electrostatic measures, however, ground all the leads on the device before blowing off the dust.
- The contamination on the glass surface should be wiped off with a clean applicator soaked in Isopropyl alcohol. Wipe slowly and gently in one direction only.

— Frequently replace the applicator and do not use the same applicator to clean more than one device.

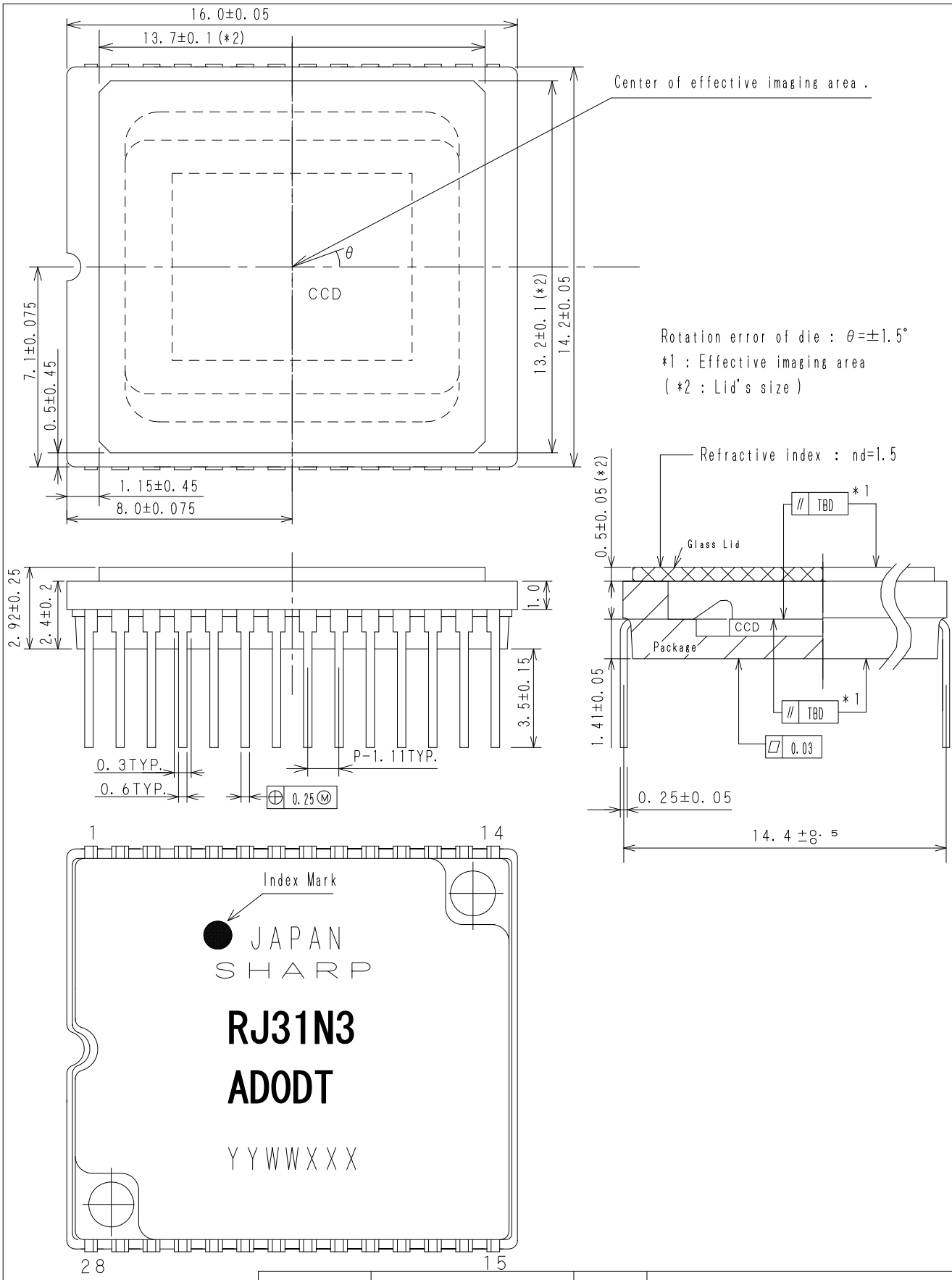
※ Note: In most cases, dust and contamination are unavoidable, even before the device is first used. It is, therefore, recommend that the above procedures should be taken to wipe out dust and contamination before using the device.

10.4 Other

1) Soldering should be manually performed within 5 seconds at 350℃ maximum at the tip of soldering iron.

2) Avoid using or storing the CCD at high temperature or high humidity as it is a precise optical component. Do not give a mechanical shock to the CCD.

3) Do not expose the device to strong light. For the color device, long exposure to strong light will fade the color of the color filters.



(UNIT : mm)

材質 MATERIAL	仕上 FINISH	名称 NAME	WDIP28-P-560 Package Outline Specification
		コード CODE	
Assembly Process Production Engineering Dept.			
ELECTRONIC COMPONENTS AND DEVICES GROUP		図番 DRAWING No.	GDP028J-01X0
SHARP CORPORATION			